Application Note AN-978

HV Floating MOS-Gate Driver ICs

(HEXFET is a trademark of International Rectifier)

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1. GATE DRIVE REQUIREMENTS OF HIGH-SIDE DEVICES

The gate drive requirements for a power MOSFET or IGBT utilized as a high-side switch (the drain is connected to the high voltage rail, as shown in Figure 1) driven in full enhancement (i.e., lowest voltage drop across its terminals) can be summarized as follows:

1. Gate voltage must be 10 V to 15 V higher than the source voltage. Being a high-side switch, such gate voltage would have to be higher than the rail voltage, which is frequently the highest voltage available in the system.
2. The gate voltage must be controllable from the logic, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the high-side power device, which, in most applications, swings between the two rails.
3. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency.

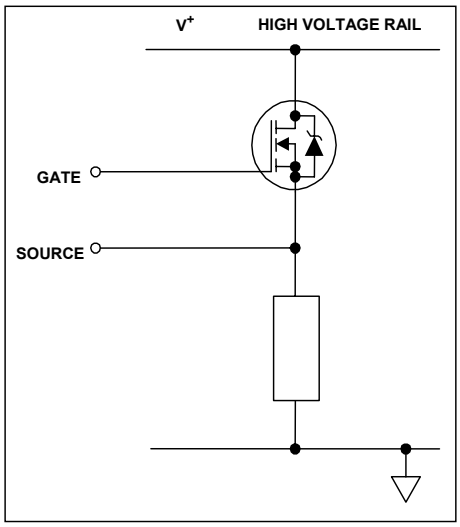


Figure 1: Power MOSFET in the High-Side Configuration

With these constraints in mind, several techniques are presently used to perform this function, as shown in principle in Table I (see pg. 29). Each basic circuit can be implemented in a wide variety of configurations.

International Rectifier's family of MOS-gate drivers (MGDs) integrate most of the functions required to drive one high-side and one low-side power MOSFET or IGBT in a compact, high performance package. With the addition of few components, they provide very fast switching speeds, as shown in Table II (see pg. 30) for the IRS2110, and low power dissipation. They can operate on the bootstrap principle or with a floating power supply. Used in the bootstrap mode, they can operate in most applications from frequencies in the tens of Hz up to hundreds of kHz.

2. TYPICAL BLOCK DIAGRAM

The block diagram of the IRS2110 will be used to illustrate the typical structure of most MGDs; this is shown in Figure 2. It comprises a drive circuit for a ground referenced power transistor, another for a high-side one, level translators and input logic circuitry

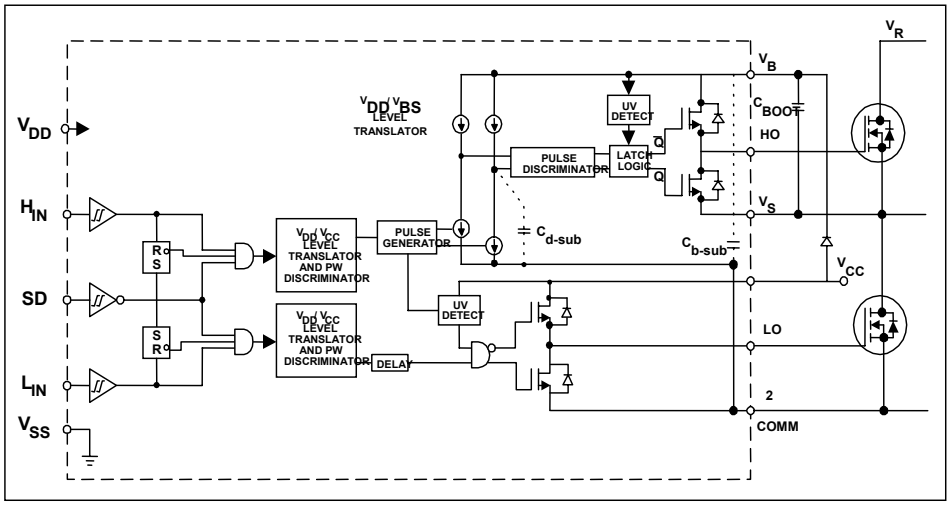


Figure 2: Block Diagram of the IRS2110

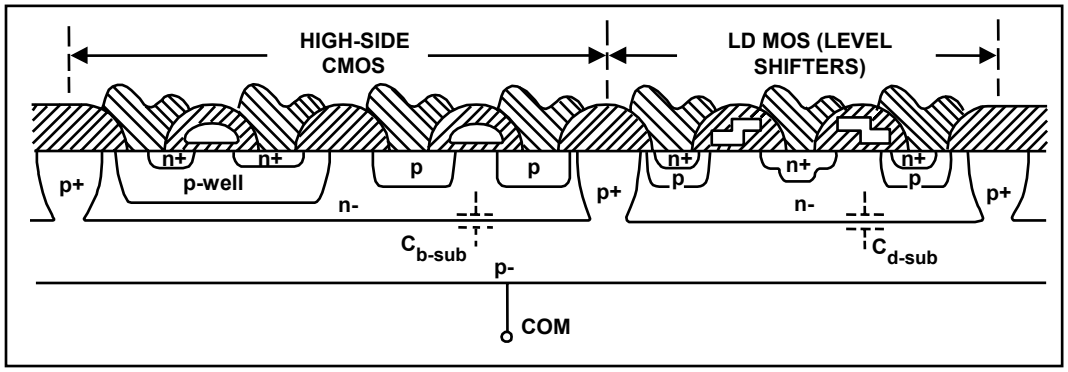


Figure 3: Silicon Cross-Section Showing the Parasitic Capacitances

2.1 Input Logic

Both channels are controlled by TTL/CMOS compatible inputs. The transition thresholds are different from device to device. Some MGDs, (e.g., IRS211x) have the transition threshold proportional to the logic supply V_{DD} (3 to 20 V) and Schmitt trigger buffers with hysteresis equal to 10% of V_{DD} to accept inputs with long rise time. Other MGDs (e.g., IRS210x, IRS212x, and IRS213x devices) have a fixed transition from logic 0 to logic 1 between 1.5 V to 2 V. Some MGDs can drive only one high-side power device (e.g., IRS2117, IRS2127, and IRS21851). Others can drive one high-side and one low-side power device. Others can drive a full three-phase bridge (e.g., the IRS213x and IRS263x families). It goes without saying that any high-side driver can also drive a low-side device. Those MGDs with two gate drive channel can have dual, hence independent, input commands or a single input command with complementary drive and predetermined deadtime.

Those applications that require a minimum deadtime should use MGDs with integrated deadtime (half-bridge driver) or a high- and low-side driver in combination with passive components to provide the needed deadtime, as shown in Section 12. Typically, the propagation delay between input command and gate drive output is approximately the same for both channels at turn-on as well as turn-off (with temperature dependence as characterized in the datasheet). For MGDs with a positive high shutdown function (e.g., IRS2110), the outputs are shutdown internally, for the remainder of the cycle, by a logic 1 signal at the shut down input.

The first input command after the removal of the shutdown signal clears the latch and activates its channel. This latched shutdown lends itself to a simple implementation of a cycle-by-cycle current control, as exemplified in Section 12. The signals from the input logic are coupled to the individual channels through high noise immunity level translators. This allows the ground reference of the logic supply (V_{SS}) to swing by ±5 V with respect to the power ground (COM). This feature is of great help in coping with the less than ideal ground layout of a typical power conditioning circuit. As a further measure of noise immunity, a pulse-width discriminator screens out pulses that are shorter than 50 ns or so.

2.2 Low-Side Channel

The driver's output stage is implemented either with two n-channel MOSFETs in the totem pole configuration (source follower as a current source and common source for current sinking), or with an n-channel and a p-channel CMOS inverter stage. Each MOSFET can sink or source gate currents from 0.12 A to 4 A, depending on the MGD. The source of the lower driver is independently brought out to the COM pin so that a direct connection can be made to the source of the power device for the return of the gate drive current. The relevance of this will be seen in Section 5. An undervoltage lockout prevents either channel from operating if V_{CC} is below the specified value (typically 8.6/8.2 V).

Any pulse that is present at the input pin for the low-side channel when the UV lockout is released turns on the power transistor from the moment the UV lockout is released. This behavior is different from that of the high-side channel, as we will see in the next subsection.

2.3 High-Side Channel

This channel has been built into an "isolation tub" (Figure 3) capable of floating from 500 V or 1200 V to -5 V with respect to power ground (COM). The tub "floats" at the potential of V_S. Typically this pin is connected to the source of the high-side device, as shown in Figure 2 and swings with it between the two rails.

If an isolated supply is connected between V_B and V_S, the high-side channel will switch the output (HO) between the positive of this supply and its ground in accordance with the input command.

One significant feature of MOS-gated transistors is their capacitive input characteristic (i.e., the fact that they are turned on by supplying a charge to the gate rather than a continuous current). If the high-side channel is driving one such device, the isolated supply can be replaced by a bootstrap capacitor (C_{BOOT}), as shown in Figure 2.

The gate charge for the high-side MOSFET is provided by the bootstrap capacitor which is charged by the 15 V supply through the bootstrap diode during the time when the device is off (assuming that V_S swings to ground during that time, as it does in most applications). Since the capacitor is charged from a low voltage source the power consumed to drive the gate is small. The input commands for the high-side channel have to be level-shifted from the level of COM to whatever potential the tub is floating at which can be as high as 1200 V. As shown in Figure 2 the on/off commands are transmitted in the form of narrow pulses at the rising and falling edges of the input command. They are latched by a set/reset flip-flop referenced to the floating potential.

The use of pulses greatly reduces the power dissipation associated with the level translation. The pulse discriminator filters the set/reset pulses from fast dv/dt transients appearing on the V_S node so that switching rates as high as 50 V/ns in the power devices will not adversely affect the operation of the MGD. This channel has its own undervoltage lockout (on some MGDs) which blocks the gate drive if the voltage between V_B and V_S (i.e., the voltage across the upper totem pole) is below its limits. The operation of the UV lockout differs from the one on V_{CC} in one detail: the first pulse *after* the UV lockout has released the channel changes the state of the output. The high voltage level translator circuit is designed to function properly even when the V_S node swings below the COM pin by a voltage indicated in the datasheet (typically 5 V). This occurs due to the forward recovery of the lower power diode or to the LdI/dt induced voltage transient. Section 5 gives directions on how to limit this negative voltage transient.

2.4 Supply Clamp

Many of the MGDs feature integrated supply clamps of 20 V or 25 V to protect against supply transients. Exceeding this clamp voltage for a substantial period of time will cause irreversible damage to the control IC.

3. HOW TO SELECT THE BOOTSTRAP COMPONENTS

As shown in Figure 2, the bootstrap diode and capacitor are the only external components strictly required for operation in a standard PWM application. Local decoupling capacitors on the V_{CC} (and digital) supply are useful in practice to compensate for the inductance of the supply lines.

The voltage seen by the bootstrap capacitor is the V_{CC} supply only. Its capacitance is determined by the following constraints:

1. Gate voltage required to enhance MGT
2. I_{QBS} - quiescent current for the high-side driver circuitry
3. Currents within the level shifter of the control IC
4. MGT gate-source forward leakage current
5. Bootstrap capacitor leakage current

Factor 5 is only relevant if the bootstrap capacitor is an electrolytic capacitor, and can be ignored if other types of capacitor are used. Therefore it is always better to use a non-electrolytic capacitor if possible. For more detailed information on bootstrap component selection see *DT98-2a "Bootstrap Component Selection for Control IC's."*

The minimum bootstrap capacitor value can be calculated from the following equation:

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS} - V_{Min}}$$

where:

Q_g = Gate charge of high-side FET
f = frequency of operation
$I_{Cbs\ (leak)}$ = bootstrap capacitor leakage current
$I_{qbs\ (max)}$ = Maximum V_{BS} quiescent current
V_{CC} = Logic section voltage source
V_f = Forward voltage drop across the bootstrap diode
V_{LS} = Voltage drop across the low-side FET or load
V_{Min} = Minimum voltage between V_B and V_S.
Q_{ls} = level shift charge required per cycle (typically 5 nC for 500 V/600 V MGDs and 20 nC for 1200 V MGDs)

The bootstrap diode must be able to block the full voltage seen in the specific circuit; in the circuits of Figures 25, 28 and 29 this occurs when the top device is on and is about equal to the voltage across the power rail. The current rating of the diode is the product of gate charge times switching frequency. For an IRF450 HEXFET power MOSFET operating at 100 kHz it is approximately 12 mA.

The high temperature reverse leakage characteristic of this diode can be an important parameter in those applications where the capacitor has to hold the charge for a prolonged period of time. For the same reason it is important that this diode have an ultra-fast recovery to reduce the amount of charge that is fed back from the bootstrap capacitor into the supply.

4. HOW TO CALCULATE THE POWER DISSIPATION IN AN MGD

The total losses in an MGD result from a number of factors that can be grouped under low voltage (static and dynamic) and high voltage (static and dynamic) conditions.

a) Low voltage static losses ($P_{D,q(LV)}$) are due to the quiescent currents from the low voltage supplies (e.g., V_{DD}, V_{CC} and V_{SS}). In a typical 15 V application these losses amount to approximately 3.5 mW at 25 °C and increase to approximately 5 mW at T_J = 125 °C .

b) Low voltage dynamic losses ($P_{D,SW(LV)}$) on the V_{CC} supply are due to two different components:

1. Whenever a capacitor is charged or discharged through a resistor, half of the energy that goes into charging the capacitance is dissipated in the resistor. Thus, the losses in the gate drive resistance (internal and external to the MGD) for one complete cycle is the following:

$$P_G = V \bullet Q_G \bullet f$$

For two IRF450 HEXFETs operated at 100 kHz with V_{gs} = 15 V, we have:

$$P_G = 2(15\ V)(120\ nC)(100\ kHz) = 0.36\ W$$

The factor 2 in the formula is valid in the assumption that two devices are being driven, one per channel. If V_{SS} is generated with a bootstrap capacitor/diode, this power is supplied from V_{CC}. The use of gate resistors reduces the amount of gate drive power that is dissipated inside the MGD by the ratio of the respective resistances. If the internal resistance is 6 Ω, sourcing or sinking, and if the gate resistor is 10 Ω, only 6/16 of P_G is dissipated within the MGD. These losses are not temperature dependent.

2. Dynamic losses associated with the switching of the internal CMOS circuitry can be approximated with the following formula:

$$P_{CMOS} = V_{CC} \bullet Q_{CMOS} \bullet f$$

with Q_{CMOS} between 5 and 30 nC, depending on MGD. In a typical 100 kHz application these losses would amount to tens of mW, (these losses are largely independent of temperature).

c) High voltage static losses ($P_{D,Q(HV)}$) are mainly due to the leakage currents in the level shifting stage. They are dependent on the voltage applied to the V_S pin and they are proportional to the duty cycle, since they only occur when the high-side power device is on. If V_S is kept continuously at 400 V they would typically be 0.06 mW at 25 °C and increase to approximately 2.25 mW at 125 °C. These losses would be virtually zero if V_S is grounded, as in a push-pull or similar topology.

d) High voltage switching losses ($P_{D,SW(HV)}$) comprise two terms, one due to the level shifting circuit (see Figure 2) and one due to the charging and discharging of the capacitance of the high-side p-well ($C_{b\text{-}sub}$ in Figure 3).

1. Whenever the high-side flip-flop is reset, a command to turn-off the high-side device (i.e., to set the flip-flop) causes a current to flow through the level-shifting circuit. This charge comes from the high voltage bus through the power device and the bootstrap capacitor. If the high-side flip-flop is set and the low-side power device is on, a command to reset it causes a current to flow from V_{CC}, through the diode. Thus, for a half-bridge operating from a rail voltage V_R, the combined power dissipation is:

$$(V_R + V_{CC}) \times Q_P \times f$$

where Q_P is the charge absorbed by the level shifter, and f the switching frequency of the high-side channel. Q_P is approximately 4 nC at V_R = 50 V and increases to 7 nC as the rail voltage increases to 500 V. In a typical 400 V, 100 kHz application these losses would amount to approximately 0.3 W. This includes the charging and discharging of $C_{d\text{-}sub}$. There is a third possible source for Q_P, when the high-side flip-flop is being reset (i.e., the power device is being turned on) and the low-side power device is off. In this case the charge comes from the high voltage bus, through the device capacitances and leakages or through the load. The power dissipation is somewhat higher than what would be calculated from the above expression. In a push-pull or other topology where V_S is grounded, both level shifting charges are supplied from V_{CC} with significantly lower losses.

2. In a high-side/low-side power circuit the well capacitance $C_{b\text{-}sub}$ is charged and discharged every time V_S swings between V_R and COM. Charging current is supplied by the high voltage rail through the power device and the epi resistance. Discharge occurs through

the lower device and the epi resistance. The losses incurred in charging or discharging a capacitor through a resistor is equal to QV/2, regardless of the value of resistance. However, much of these losses occur outside the bridge driver, since the epi resistance is negligible compared to the internal resistance of the power devices during their switching transitions. Assuming a charge value of 7 nC at 450 V and an operating frequency of 100 kHz, the *total* losses caused by the charging and discharging of this capacitance amount to:

$$P_{Total} = V \times Q \times f = 450\ V(7\ nC)(100\ kHz) = 0.31\ W$$

If V_S is grounded the capacitor is charged at a fixed voltage and these losses would be zero. $C_{b\text{-}sub}$ (like $C_{d\text{-}sub}$) is a reverse biased junction and its capacitance is a strong function of voltage. These charges are not temperature dependent.

The above discussion on losses can be summarized as follows:

- The dominant losses are switching and, in high voltage applications at 100 kHz or above, the static losses in a) and c) can be neglected outright.
- The temperature dependence of the switching losses is not significant;
- The combined losses are a function of the control mode, as well as the electrical parameters and temperature.

Knowing the power losses in the MGD, the maximum ambient temperature can be calculated (and vice-versa) from the following expression:

$$T_{A,max} = T_{J,max} - PD \times R_{th,JA}$$

where $R_{th,JA}$ is the thermal resistance from die to ambient.

The following example shows a typical breakdown of losses for two IRF830s in a half-bridge, from a 400 V rail, 100 kHz, no load, and no gate resistors.

$P_{D,q(LV)} = 0.004\ W$

$P_{D,SW(LV)} = P_{CMOS} = (15\ V)(16\ nC)(100\ kHz) = 0.024\ W$

$P_G = 2(15\ V)(28\ nC)(100\ kHz) = 0.084\ W$

$P_{D,q(HV)} = 0.002\ W$

$P_{D,SW(HV)} = (400\ V + 200\ V)(7\ nC)(100\ kHz) = 0.42\ W$

Total power loss = 0.534 W

The value of 200 V in the formula to calculate $P_{D,SW(HV)}$ is appropriate at no load, i.e., the output of the half-bridge settles on a voltage that is between the two rails (See Section 4.2.d.1)

The actual junction temperature can be measured while in operation by pulling 1 mA from the shutdown pin with the help of an adjustable current source (like the LM334). The voltage at the pin is 650 mV at 25 °C, decreasing by 2 mV/°C. Changes in this voltage are a reasonable indication of the temperature of the die.

5. HOW TO DEAL WITH NEGATIVE TRANSIENTS ON THE V_S PIN

Of the problems caused by parasitics, one of the main issues for control ICs is a tendency for the V_S node to undershoot the ground following switching events. Conversely, overshoot does not generally present a problem due to the high differential voltage capability of International Rectifier's proven HVIC process.

International Rectifier's control ICs are guaranteed to be completely immune to V_S undershoot of at least 5 V, measured with respect to COM. If undershoot exceeds this level, the high-side output will temporarily latch in its current state. Provided V_S remains within absolute maximum limits the IC will not suffer damage, however the high-side output buffer will not respond to input transitions while undershoot persists beyond 5 V. This mode should be noted but proves trivial in most applications, as the high-side is not usually required to change state immediately following a switching event.

The signals listed below should be observed both in normal operation and during high-stress events such as short circuit or over-current shutdown, when di/dt is highest. Readings should always be taken directly across IC pins as shown in Figure 4, so that contributions from the parasitics in the drive coupling are included in the measurement.

(1) High-side offset with respect to common; V_S-COM
(2) The floating supply; V_B - V_S

The following guidelines represent good practice in control IC circuits and warrant attention regardless of the observed latch-up safety margin.

5.1 Minimize the parasitics

1a. Use thick, direct tracks between switches with no loops or deviation.
1b. Avoid interconnect links. These can add significant inductance.
1c. Reduce the effect of lead-inductance by lowering package height above the PCB.
1d. Consider co-locating both power switches to reduce track lengths.

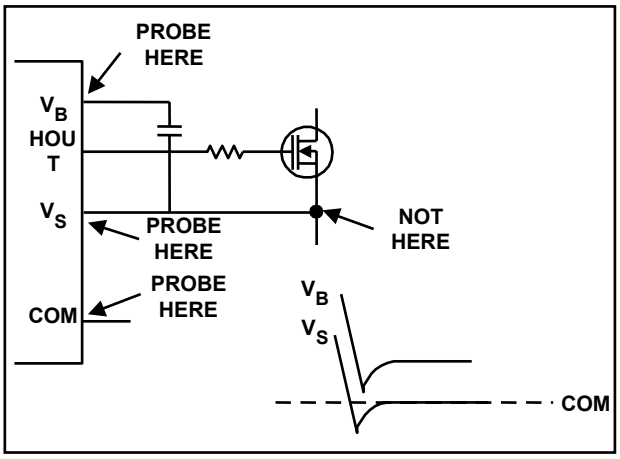


Figure 4: Considering the V_S Spike During the Reverse Recovery

5.2 Reduce control IC exposure

2a. Connect V_S and COM as shown in Figure 6.
2b. Minimize parasitics in the gate drive circuit by using short, direct tracks.
2c. Locate the control IC as close as possible to the power switches.

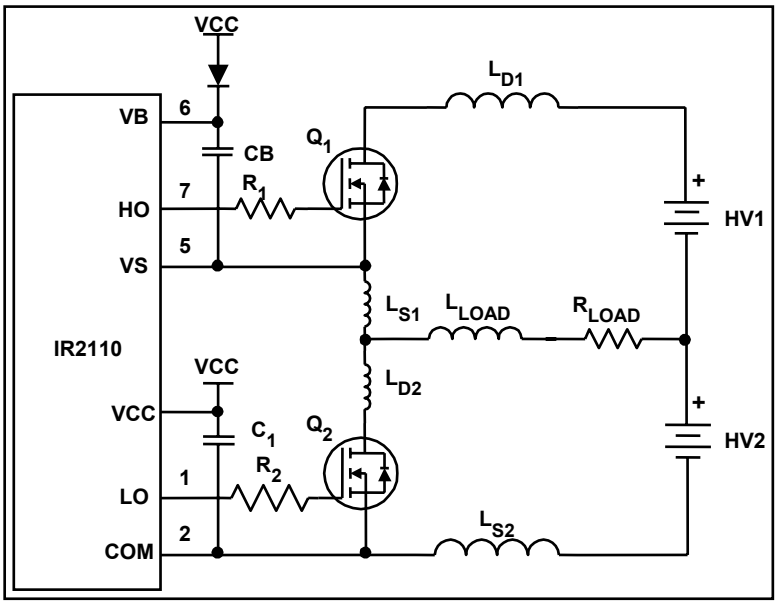


Figure 5A: Typical Half-Bridge Circuit with Stray Inductances

Improve local decoupling.

3a. Increase the bootstrap capacitor (C_B) value to above 0.47 μF using at least one low-ESR capacitor. This will reduce overcharging from severe V_S undershoot.
3b. Use a second low-ESR capacitor from V_{CC} to COM. As this capacitor supports both the low-side output buffer and bootstrap recharge, we recommend a value at least ten times higher than C_B.
3c. Connect decoupling capacitors directly across the appropriate pins as shown in Figure 7.
3d. If a resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM, especially during start-up and extremes of frequency and duty cycle.

Granted proper application of the above guidelines, the effects of V_S undershoot will be minimized at source. If the level of undershoot is still considered too high, then some reduction of dv/dt may be necessary.

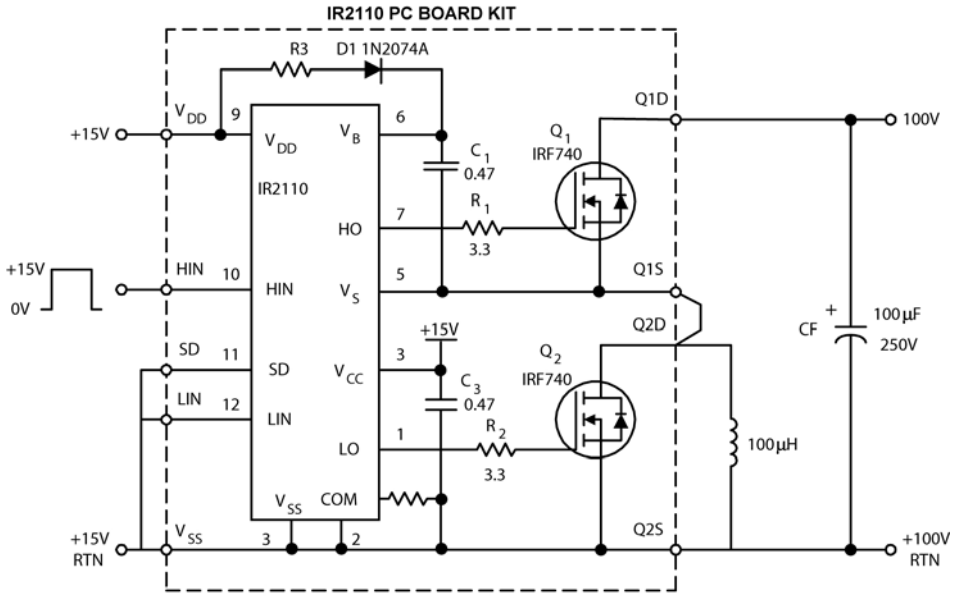


Figure 5B: Test Circuit

External snubbing and/or increasing gate drive resistance may be used to trade efficiency for lower switching rate. If the system will not tolerate this, then fast anti-parallel clamping diodes may be considered appropriate. HEXFRED diodes are ideal for this purpose.

For More detailed information on managing transients see *DT97-3 "Managing Transients in Control IC Driven Power Stages."*

6. LAYOUT AND OTHER GENERAL GUIDELINES

A typical half-bridge circuit is shown in Figure 5a with its stray inductances. It shows critical stray inductances located in the high current path; these stray inductances can affect the operation of the circuit. L_{D1} and L_{S2} are in a "DC path" and are due to the wiring inductance between the MOSFETs and the decoupling capacitors; L_{S1} and L_{D2} are in an "AC path" and are due to the wiring inductance between the MOSFETs. The stray inductance in a DC path can be cancelled with a capacitor; those in an AC path cannot be compensated for.

To eliminate the effects of the inductance of the wiring between the power supply and the test circuit, a 100 uF/250 V electrolytic capacitor was connected between Q1D and Q2S terminals, as shown in Figures 6 and 7. This virtually eliminates any stray inductance in the dc path.

The associated waveforms are shown in Figure 8. When Q1 turns off, the body diode of Q2 carries the freewheeling current. The voltage spike across the freewheeling diode is approximately 10 V, as shown in the top trace, due to the forward recovery of the diode and the internal packaging inductances.

However, the corresponding negative spike at the V_S pin of the IR2110 is 50 V, as shown by the lower trace. This is caused by the di/dt in the stray inductances L_{D2} and L_{S2} in the ac path and the fact that these inductances effectively isolate the V_S pin from the clamping action of the freewheeling diode. The severity of the problem can be understood considering that by switching 10 A in 20 ns with a stray inductance of 50 nH, a 25 V spike is generated. As a point of reference, small paper clip has an inductance of 50 nH.

The most effective way of dealing with this spike is to reduce the stray inductance in the AC path. This can be done by mounting the source or emitter of the high-side device very close to the drain or collector of the low-side device, as shown in the layout of Figure 10.

After this inductance has been reduced to the lowest practical limit, the di/dt may have to be reduced by reducing the switching speed by means of the gate resistor. Driving MOS-gated power transistors directly from the MGDs can result in unnecessarily high switching speeds. The circuit shown in Figure 5b produced 4 ns turn-off time with 0 ohm series gate resistance and generated a negative spike of 90 V at the V_S pin (IR2110 waveform). A graph of the negative spike and the turn-off time versus series gate resistance is shown in Figure 9.

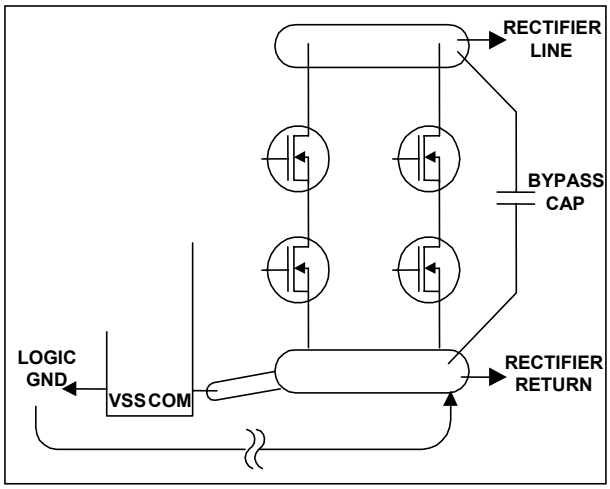


Figure 6: Ground Connections and Layout

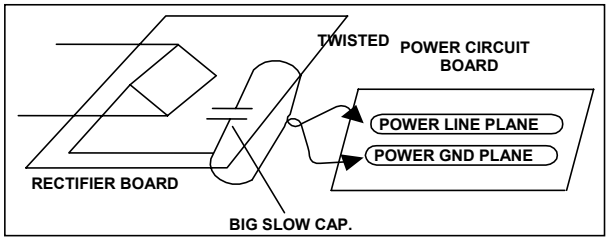


Figure 7: Power Bypass Capacitor

Increasing the value of the series gate resistor, results in a rapid decrease of the amplitude of the negative spike, while the turn-off time is a linear function of the series gate resistance. Selecting a resistor value just right from the “knee” in Figure 9 provides a good trade-off between the spike amplitude and the turn-off speed. A 27 Ω speed gate resistor was selected for the test circuit which resulted in an 18 V spike amplitude and set the turn-off time to 48 ns. A parallel diode, with the anode towards the gate, across the gate resistor is also recommended. The diode is reverse biased at turn-on but holds the gate down at turn-off, and during the off state. The reduction in the turn-on speed reduces the spike of reverse recovery, as explained in Section 12 (see also Reference 2). The value of the gate resistor should be as low as the layout allows, in terms of overvoltage on the device and negative spikes on the V_S pin.

The layout should also minimize the stray inductance in the charge/discharge loops of the gate drive to reduce oscillations and to improve switching speed and noise immunity, particularly the "dV/dt induced turn-on". To this end, each MOSFET should have a dedicated connection going directly to the pin of the MGD for the return of the gate drive signal. Best results are obtained with a twisted pair connected, on one side, to gate and source, on the other side, to gate drive and gate drive return.

The layout shown in Figure 10 reduces the stray inductances in the AC path, in the DC path, as well as the stray inductance in the gate drive loop. Parallel tracks on the PC board are to be used. In this circuit the voltage differential measured between the gate pin of the power MOSFET and the drive pin of the IR2110 during a fast transient was in excess of 2 V.

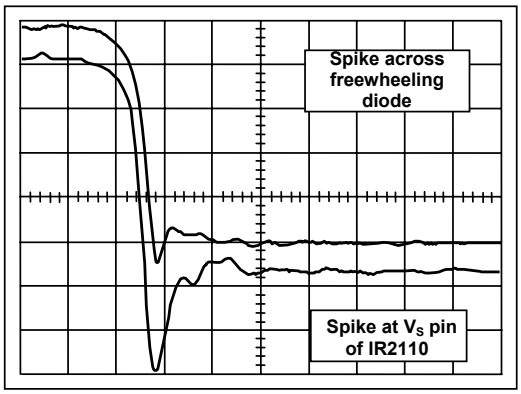


Figure 8: Q1 Turning Off a 20 A Inductive Load (20 ns / div and 20 V / div)

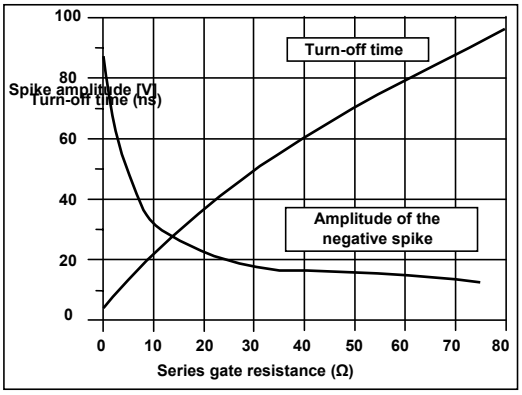


Figure 9: Series Gate Resistance vs. Amplitude of Negative Voltage Spike and Turn-off time

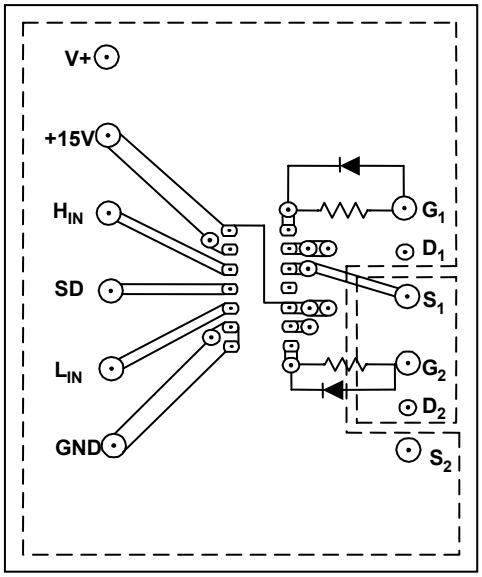


Figure 10: IR(S)2110 Test Circuit

7. HOW TO BOOST GATE DRIVE CURRENT TO DRIVE MODULES

Modules and other paralleled MOS-gated power transistors at times require more current and lower gate drive impedance than what a typical MGD can provide. The high input impedance power buffer shown in Figure 11 delivers 8 A peak output current. It can be mounted close to the power module, thus reducing the inductance of the gate drive loop and improving the immunity to dv/dt induced turn-on. It draws negligible quiescent current and can still be supplied by a bootstrap capacitor. The buffer receives its drive signal from the IRS2110 or an MGD with lower gate drive capability, and drives an IGBT module which has a total gate charge of 600 nC. Q1 and Q2 are low current drivers for Q3 and Q4 which can be sized to suit the peak output current requirement. When the input signal changes state, R1 limits the current through Q1 and Q2 for the few nanoseconds that both transistors are on. When the input settles to its new state, the driver transistor quickly discharges the gate capacitance of the conducting output transistor forcing it into off-state. Meanwhile the gate of the other output transistor will be charged through R1; the turn-on will be delayed by the RC time constant formed by R1 and the input capacitance of the output transistor.

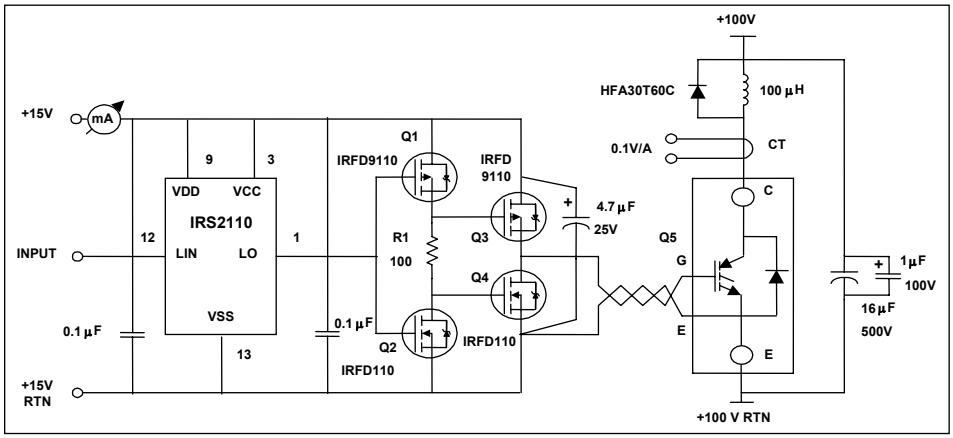


Figure 11: Test Circuit

The typical switching performance while driving an inductive load current of 60 A is shown in Figures 12A and 12B. Turn-on and turn-off delays are 50 ns. Rise and fall times are less than 40 ns. The buffer was tested with a 0.1uF capacitive load; the input and output buffer waveforms are shown in Figure 13. The ringing was due to the resonant circuit at the output, formed by the capacitive load and the stray inductances. The current consumption vs. frequency plot is shown in Figure 14. It is possible to use lower on-resistance, lower voltage HEXFETs in the booster stage, but it was found that the large reduction in $R_{DS(on)}$ gave rise to large peak currents which can cause a higher noise and ringing in the circuit.

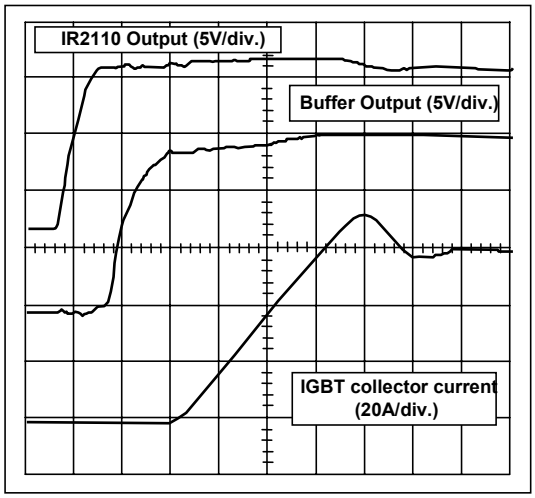


Figure 12A: Turn-On of IGBT Module Switching 60 A Inductive Load
(50 ns / div)

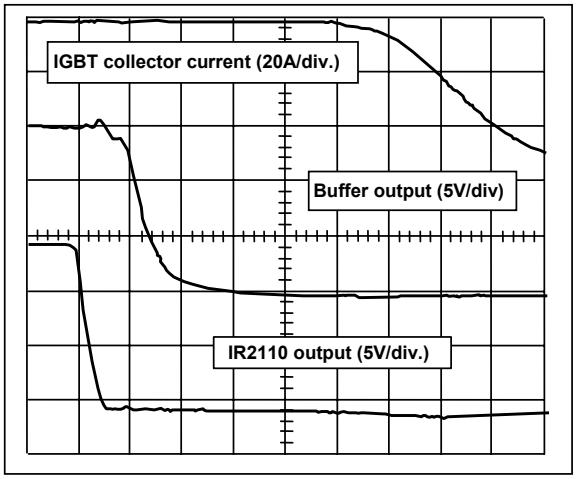


Figure 12B: Turn-Off of IGBT Module
Propagation Delay is 50 ns; Fall Time is <40 ns; Q_g is 600 nC
(50 ns / div)

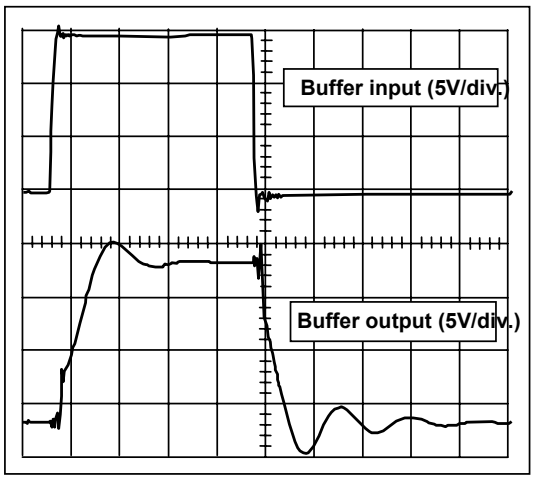


Figure 13: Waveform Driving 0.1 uF Capacitor (250 ns /div)

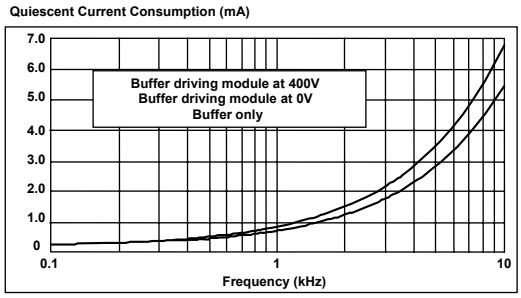


Figure 14: Current Consumption vs. Frequency

8. HOW TO PROVIDE A CONTINUOUS GATE DRIVE

Some applications, like brushless dc motors, require that the high-side device be on for an indefinite period of time. Under these conditions the charge in the bootstrap capacitor may not be adequate to keep the high side output on. Isolated supplies are normally used for this purpose.

But isolated supplies add cost and are frequently responsible for spurious turn-on of the power devices due to the coupling of the switching dv/dt through the inter-winding capacitance of their transformer. An inexpensive alternative to an isolated supply is the charge pump circuit shown in Figure 16. The IR2125 MGD was selected to demonstrate the cooperation of the charge pump and the bootstrap circuits. The IR2125 also has linear current limiting and time-out shut down capability, providing protection for the MOS-gated device. To provide the low operating current requirement of the IR2125, the charge pump employs a CMOS version of the 555 timer.

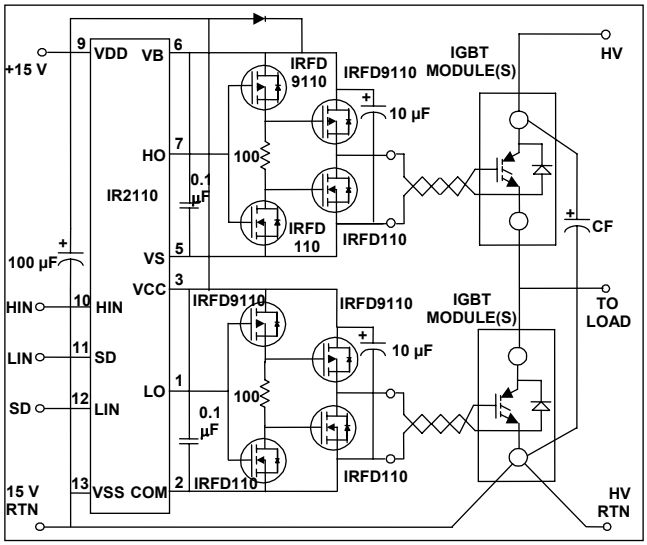


Figure 15: Application Circuit Schematic

When the IGBT is off, the bootstrap capacitor is charged through the bootstrap diode and the load resistor. When the IGBT is on, the 100 kΩ resistor connected to ground charges the 100 nF capacitor connected between pins 1 and 8 of the 555 timer generating -15 V referenced to pin 5 of the IR2125. The charge pump circuit formed by the two IN4148 diodes and the 10 nF capacitor which converts the 7.5 kHz square wave at pin 3 of the 555 timer to + 15 V referenced to V_S and charges the bootstrap capacitor.

Figure 17 shows the circuit waveforms at start-up. As the IGBT turns on, the bootstrap diode disconnects pin 8 of the IR2125 from the +12 V power supply, and the voltage across the bootstrap capacitor starts dropping. At the same time the 100 kΩ resistor located between pin 1 of the 555 timer and ground starts charging the 100 nF capacitor connected to it and generates supply voltage for the CMOS (MAXIM ICL71555IPA) timer.

The output voltage of the charge pump increases with increasing supply voltage. The charge pump maintains the voltage in the bootstrap capacitor, keeping the voltage above the undervoltage threshold level of the IR2125.

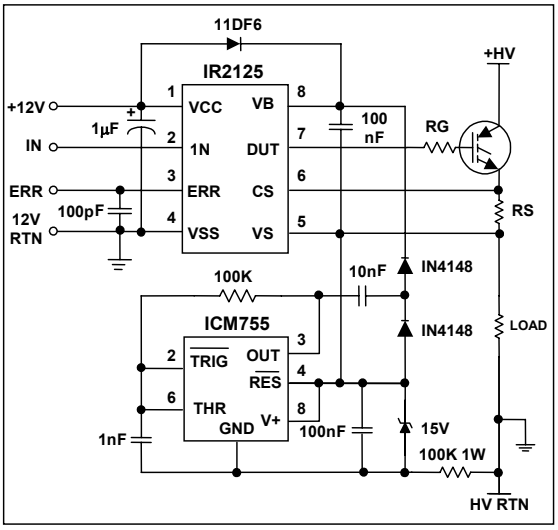


Figure 16: High-Side Drive Provides Fast Switching, Continuous On-Time and Switching Device Protection

The following considerations should be kept in mind in the selection of the components:

- In selecting the zener, consider that he absolute maximum voltage supply voltage for the 555 is 18 V
- The 100 kW (value valid for a 500 V +HV supply) resistor should be sized according to the maximum supply current at the high-side of the IR2125, the minimum operating power supply voltage and the timing requirements
- The supply current at the V_B pin (I_{QBS}) of the IR2125 increases with increasing temperature

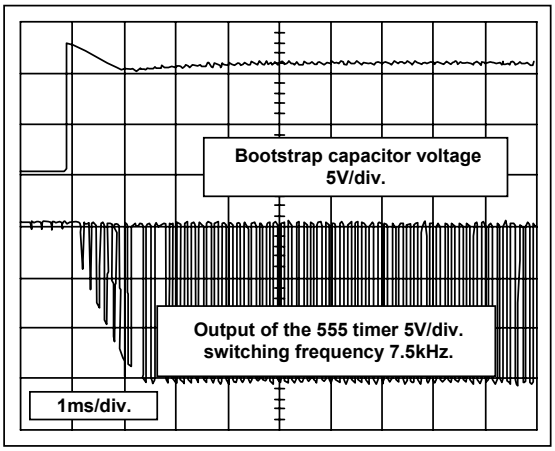


Figure 17: Waveforms at Start-Up

9. HOW TO GENERATE A NEGATIVE GATE BIAS

Inherently neither the MOSFET nor the IGBT requires negative bias on the gate. Setting the gate voltage to zero at turn-off insures proper operation and virtually provides negative bias relative to the threshold voltage of the device. However, there are circumstances when a negative gate drive or another alternative may be necessary.

- The semiconductor manufacturer specifies negative gate bias for the device,
- When the gate voltage can not be held safely below the threshold voltage due to noise generated in the circuit.
- The ultimate in switching speed is desired

Although reference will be made to IGBTs, the information contained is equally applicable to power MOSFETs. The IGBTs made by International Rectifier do not require negative bias. The switching times and energy loss values that are published on the data sheets
for both discretes and modules were measured at zero gate voltage turn-off. The problem of "dv/dt induced turn-on" arises when the voltage increases rapidly between the collector-emitter terminals of the IGBT.

During the transient, the gate-collector (Miller) capacitance delivers charge to the gate, increasing the gate voltage. The height and width of the voltage 'blip' at the gate is determined by the ratio of the gate- collector and gate-emitter capacitances, the impedance of the drive circuit connected to the gate, and the applied dv/dt between the collector-emitter terminals.

The following test was conducted to determine the threshold voltage and the effect of the series gate resistance in high dv/dt applications. The test circuit is shown in Figure 18. The positive bias to the upper IGBT was increased until the switching losses in the bottom IGBT indicated excessive shoot-through current. The turn-on loss was measured at 15 A inductor current and 6 V/ns switching speed. The results are shown in Figure 19.

The threshold voltage levels increasing the turn-on losses are 4 V, 5 V and 5.6 V with 47 ohm, 10 ohm, and 0 ohm series gate resistance, respectively. A parallel diode across the series gate resistor (anode toward the gate) helps clamp the gate low, so the series gate resistor can be sized according to the turn-on requirements.

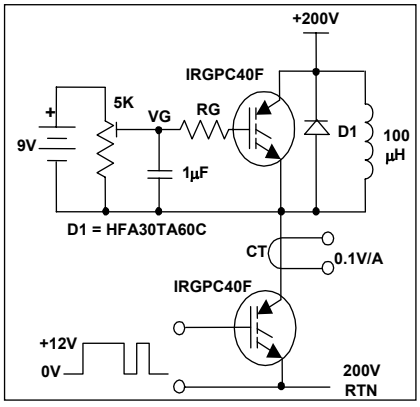


Figure 18: Test Circuit

The current 'blip' due to charging the output capacitance (C_{OES}) of the IGBT is frequently mistaken for conduction current. The amplitude of the current 'blip' is approximately 5 A for an IRGPC50F IGBT at a dv/dt of 20 V/ns. The amplitude of the 'blip' does not change with the applied negative bias.

The basic buffer circuit and the negative charge pump are shown in Figure 20. The buffer circuit employs two p-channels and two n-channel MOSFETs. Resistor R1 between the gates of Q3 and Q4 slows down the turn-on of the output transistor and limits the shoot-through current in the drivers.

D1 reduces the voltage to the gate of Q4. D2, C2 and R2 form a level shifter for Q2. C3, C4, D3 and D4 convert the incoming signal to negative DC voltage. After turn-on, the negative voltage settles in a few cycles even at extremely low or high duty cycles (1-99%). The settling time and the stiffness of the negative voltage are affected by the output impedance of the signal source.

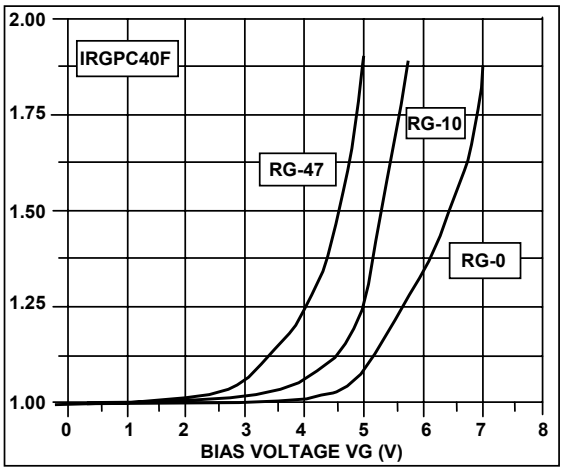


Figure 19: Turn-On Losses vs. V_g

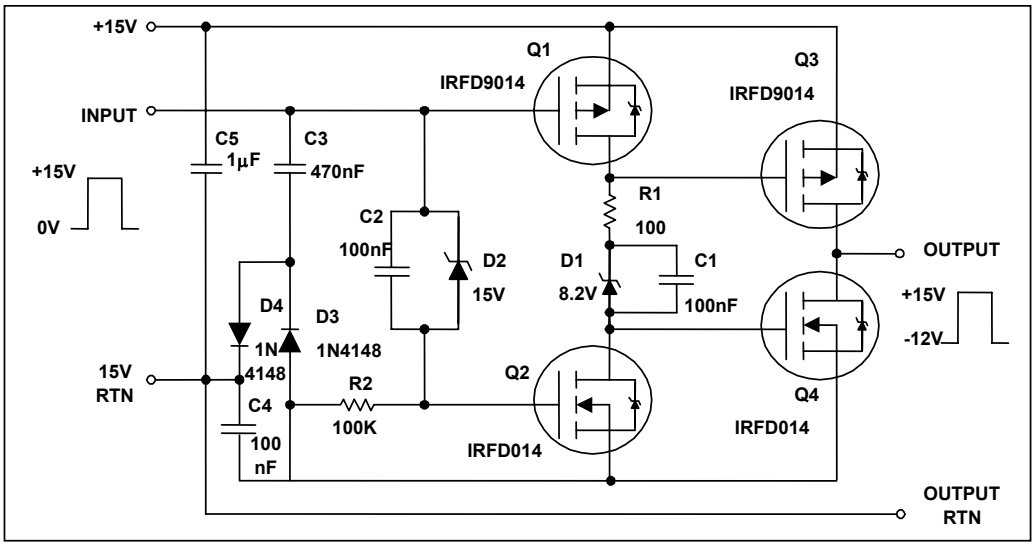


Figure 20: Buffer with Negative Charge Pump

The circuit shown in Figure 21 utilizes the high voltage level shifting capability of the IR2110 combined with the drive capability and negative bias of the MOS buffer shown in Figure 20. The circuit was tested with two 270 A IGBT modules with 600 nC of gate charge. The waveforms are shown in Figure 22. The turn-on delay of the circuit is 1 ms, the turn-off delay is 0.2 ms.

The settling time of the negative bias voltage is about 10 ms at a switching frequency of 5 kHz and at 50% duty cycle? At start-up, the circuit delivers some negative gate voltage even after the first cycle. During power down, the gate voltage remains negative until the reservoir capacitor discharges.

IMPORTANT NOTE: A negative gate drive is not required for IR IGBTs and IGBT modules. Also for NPT type IGBTs the negative gate drive is required to account for the significant change in the C_{cg} to C_{ge} capacitance ratio. It is possible to eradicate the need for negative gate drive by adding gate capacitance, which reduces the C_{cg} to C_{ge} ratio, and hence swamps out the miller effect, eliminating the false turn-on caused by the induced miller voltage on the gate.

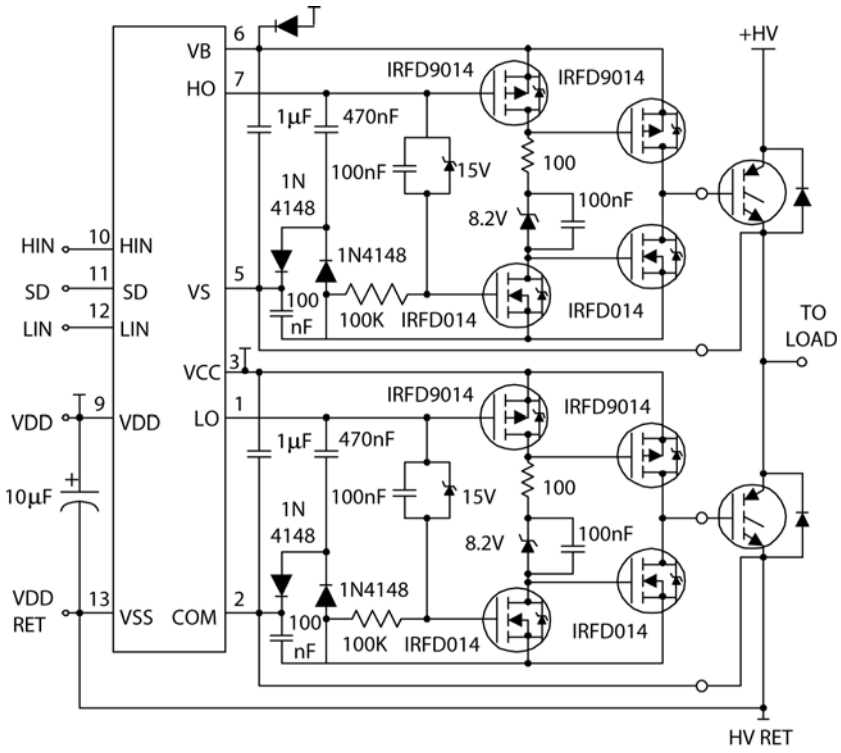


Figure 21: Half-Bridge Drive with Negative Bias

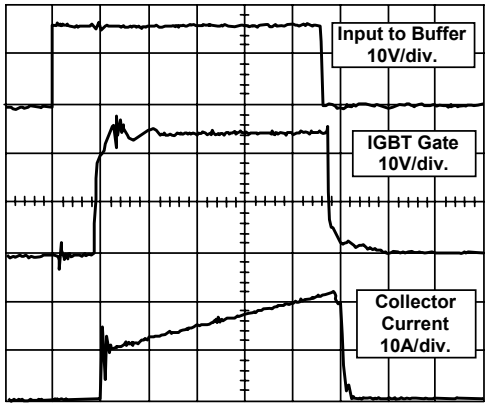


Figure 22: Waveform From Negative Bias (1 ms / div)

10. HOW TO DRIVE A BUCK CONVERTER

Figure 23 shows a typical implementation of a buck converter with the high-side drive function performed by the IR2117. The diode connected on COM prevents the negative spikes from affecting the operation of the IC and provides an extra measure of noise immunity. As mentioned before, COM *should not* be connected together.

At start-up the bootstrap capacitor is discharged and, in most applications would charge through the inductor and the filter capacitor. The same is true under no-load conditions, when the freewheeling diode may not conduct at all. This alternative path works, as long as the filter capacitor is at least 10 times larger than the bootstrap capacitor. The Q of this resonant circuit should be low enough to insure that the bootstrap capacitor does not get charged beyond the limits of V_{SS} (20 V). If this is not so, a zener in parallel with the bootstrap capacitor would take care of possible overvoltage events. This is true whether the dc-to-dc converter performs the function of a supply or speed control for a dc motor.

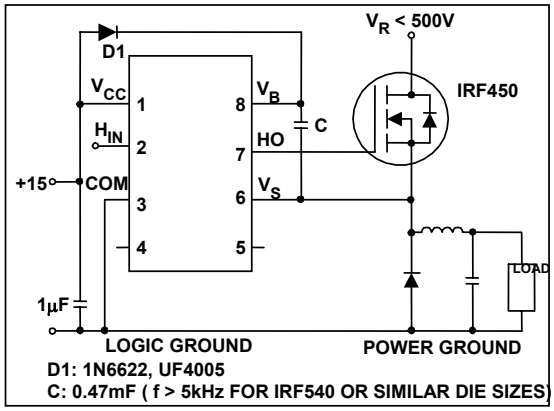


Figure 23: Buck Converter

In the following two cases, however, the recharging current for the bootstrap capacitor cannot flow either in the diode or the load:

1. In a typical battery charger application, as the one shown in Figure 24, the +12 V from the output appears at the V_S pin and reduces the voltage across bootstrap capacitor at start-up and the undervoltage protection in the MGD inhibits the operation.

2. When the regular PWM operation of the buck is interrupted due to excessive voltage at the output. This is normally due to a sudden removal of a heavy load at the output which results in higher output voltage than the set value due to the limited speed of the control loop and the stored energy in the inductor (L1). With no load or light load at the output, the filter capacitor can keep the output high for long time while the CB is being discharged at faster rate by the leakage current of the high-side driver.

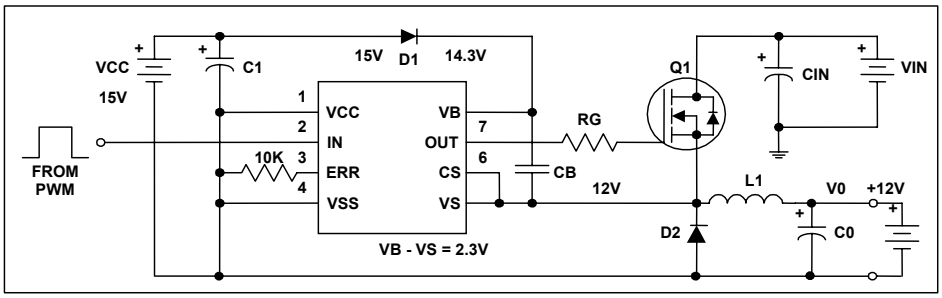


Figure 24: HVIC in Battery Charger Application

As shown in Figure 25, the addition of R1 provides an alternative charging path for the bootstrap capacitor. Because V_{IN} is higher than V_O, some charging current always flows through R1 even if V_S pin is sitting at V_O potential.

To keep CB charged the average current through R1 should be higher than the worst case leakage current. D3 should be a low level zener diode with sharp knee at low currents. The recommended part numbers for 12 V and 15 V are respectively: IN4110 and IN4107.

This technique can also be used in place of a dedicated supply to power the PWM controller, as well as the IR2110 and other auxiliary circuits, if the output voltage of the buck converter is between 10 and 20 V.

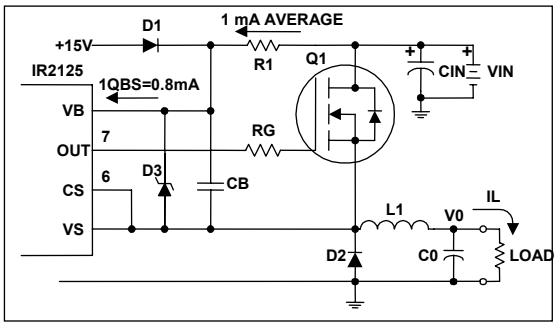


Figure 25: Adding R1 to the Circuit

11. DUAL FORWARD CONVERTER AND SWITCHED RELUCTANCE MOTOR DRIVES

Figure 26 shows a bridge arrangement that is frequently used to drive the windings of a switched reluctance motor or a transformer in a dual forward converter.

The use of the IR2110 requires the addition of two diodes and two MOSFETs to insure that the bootstrap capacitor is charged at turn on and in subsequent cycles, should the conduction time of the freewheeling diodes become very short.

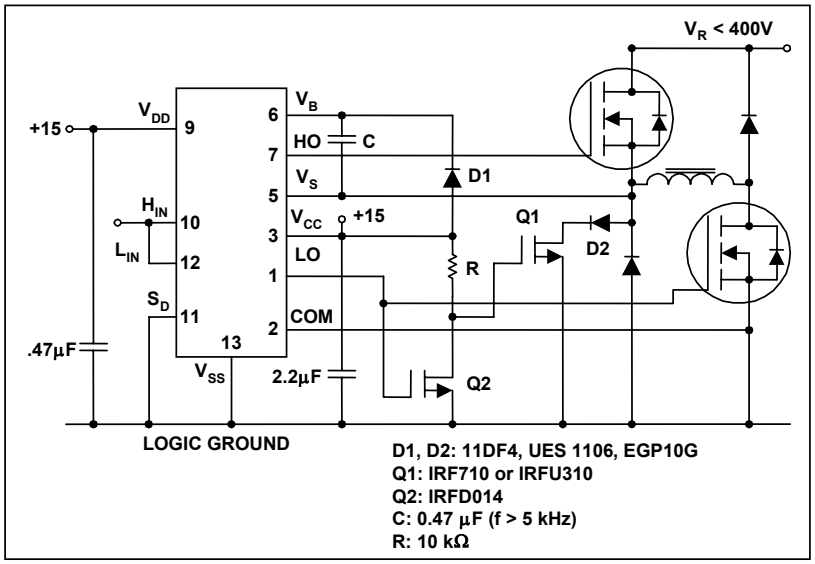


Figure 26: Dual Forward Converter and Switched Reluctance Motors

12. FULL BRIDGE WITH CURRENT MODE CONTROL

Figure 27 shows an H-bridge with cycle-by-cycle current control implemented with current sensing devices on the low-side in combination with the shutdown pin of the IR2110. The detailed implementation of the current sensing circuit is dependent on the PWM technique used to generate the desired output voltage, the accuracy required, the availability of a negative supply, bandwidth, etc. (Ref. 3, 4 and 5 cover these aspects in greater detail). As explained in Section 2.1, the shutdown function is latched so that the power MOSFETs will remain in the off-state as the load current decays through their internal diodes. The latch is reset at the beginning of next cycle, when the power devices are once again commanded on. As shown in Figures 6 and 7, decoupling capacitors mitigate the negative effects of L1. L2, on the other hand, must be reduced with a tight layout, as per Figure 10. The turn-on and turn-off propagation delays of the IR2110 are closely matched (worst case mismatch: 10 ns), with the turn-on propagation delay 25 ns longer than the turn-off. This, by itself, should insure that no conduction overlap of the power devices would occur, even if the on and off input command coincide.

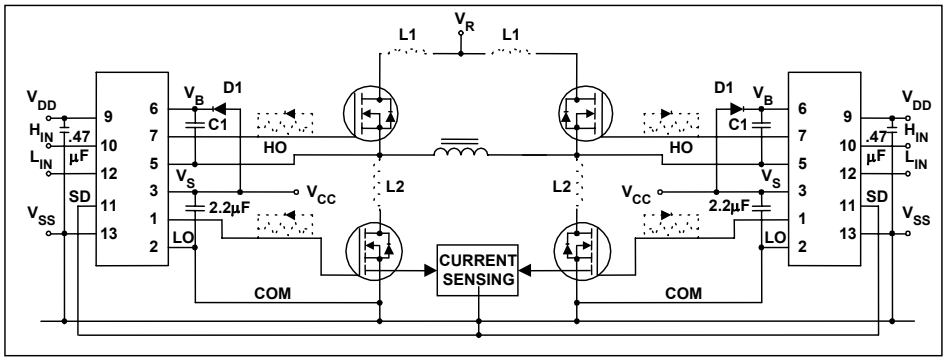


Figure 27: Typical Implementation of an H-bridge with Cycle-By-Cycle Current Mode Control

As an added safety margin a resistor diode network can be added to the gate, as shown with dashed lines in Figure 28A. The purpose of this network is to further delay the turn-on, without affecting the turn-off, thereby inserting some additional dead-time. The resistor-diode network is also useful in reducing the peak of the current spike during the reverse recovery time. As explained in Ref. 2, this has an impact on power losses, as well as dv/dt and EMI. Figures 28A & 28B show the waveforms taken from a test circuit laid out as shown in Figure 10. Operation at 500 kHz with the IRF830 HEXFET did not present any problem nor cause any noticeable heating of the IR2110.

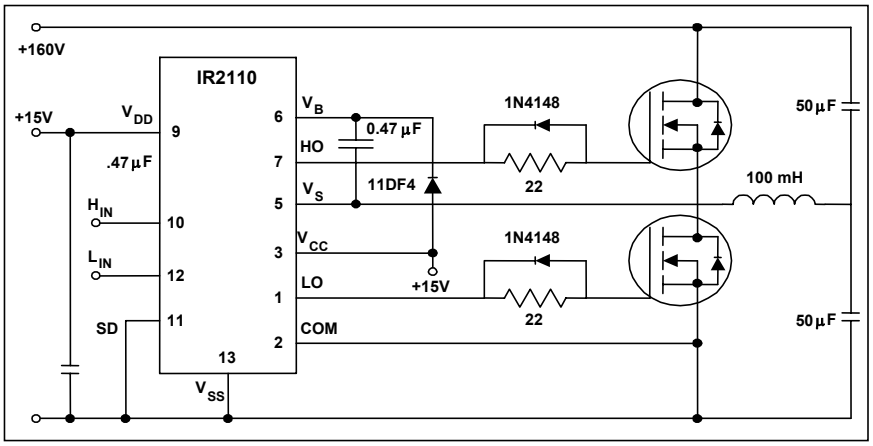


Figure 28A: IRF450 Operated at Approximately 100 kHz in a 100 mH inductor

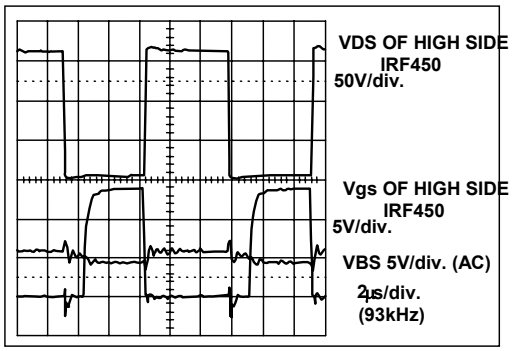


Figure 28B: Waveform for Circuit in Figure 28A

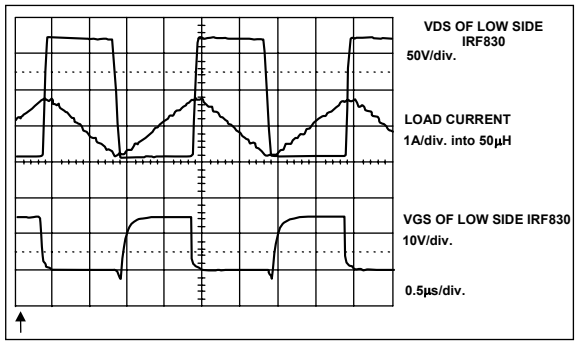


Figure 28C: Waveform for Circuit in Figure 28A

13. BRUSHLESS AND INDUCTION MOTOR DRIVES

The implementation of a three-phase bridge for motor drives requires a more careful attention to the layout due to the large di/dt components in the waveforms. In particular, the driver furthest away from the common grounding point will experience the largest voltage differential between COM and the ground reference (Ref. 1).

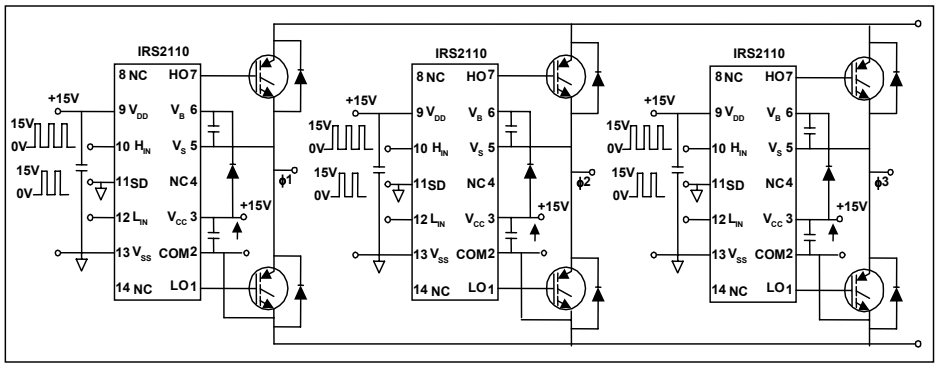


Figure 29: Three-Phase Inverter Using Three IRS2110 Devices to Drive Six IGBTs

In the case of the three-phase drivers, like the IR213x, the guidelines of Sections 5 and 6 should be complemented with the following: Three separate connections should go from the COM pin of the MGD to the three low-side devices. Furthermore, there are several operating conditions that require close scrutiny as potential problem areas.

One such condition could occur when a brushless dc motor is operated with locked rotor for an indefinite period of time with one leg of the bridge being off.

In this condition the bootstrap capacitor could eventually discharge, depending on the voltage seen by V_S during this period of time. As a result the top power device would shut off and would not go on when commanded to do so. In most cases this would not be a cause for malfunction, since the lower device would be commanded on next and the bootstrap capacitor would be charged and ready for next cycle. In general, if the design cannot tolerate this type of operation, it can be avoided in one of four ways:

a. a charge pump could be implemented, as described in Section 8;

b. the control could be arranged to have a very short “normal” duty cycle with a minimum pulse width of a couple of microseconds;

c. if a pole can be inactive for a limited and known period of time, the bootstrap capacitor could be sized to hold up the charge for that time.

d. Isolated supplies could be provided for the high-side, in addition to the bootstrap capacitor.

If the bridge is part of an induction motor drive that use a PWM technique to synthesize a sine wave, each pole goes through prolonged periods of time with zero or very low duty cycle at low frequency. The bootstrap capacitor should be sized to hold enough charge to go through these periods of time without refreshing. In circuits like the one shown in Figure 31, galvanic isolation between the high voltage supply and the logic circuitry is frequently mandated by safety considerations or desirable as a form of damage containment in case of inverter failure.

Optoisolators or pulse transformers are frequently used to perform this function. For drives up to 5 kW, the circuit shown in AN-985 is probably the simplest and most cost-effective way of providing isolation. The use of an MGD shields the optoisolator from the high-voltage dV/dt and reduces their cost while providing a high performance gate drive capability.

14. PUSH-PULL

High-voltage MGDs can still make a very useful contribution in applications that do not capitalize on their key feature, the high voltage level shifting and floating gate drive.

Convenience, noise resilience between V_{SS} and COM and high speed drive capability are appealing features in most power conditioning applications. They can perform the interface and gate drive function with the simple addition of the decoupling capacitors, as shown in Figure 30.

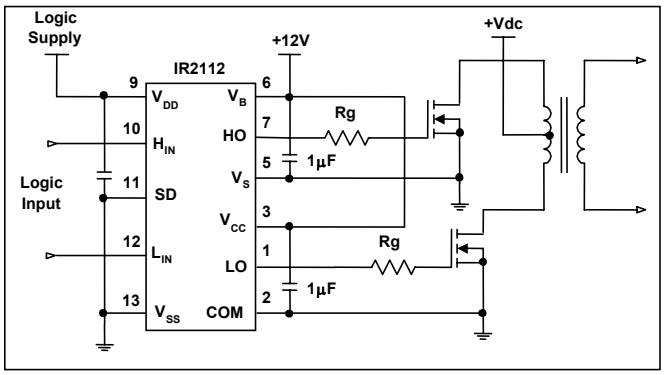


Figure 30: Push-Pull Drive Circuit

15. HIGH-SIDE P-CHANNEL

MGDs can also drive a P-Channel device as a high-side switch, provided that a negative supply referenced to the positive rail is available, as shown in Figure 31. When operated in this mode, the H_{IN} input becomes active low, i.e., a logic 0 at the input turns on the p-channel MOSFET. Whenever V_S (or V_B) are at fixed potential with respect to ground, the power losses mentioned in Section 4.2.d.2 would be zero.

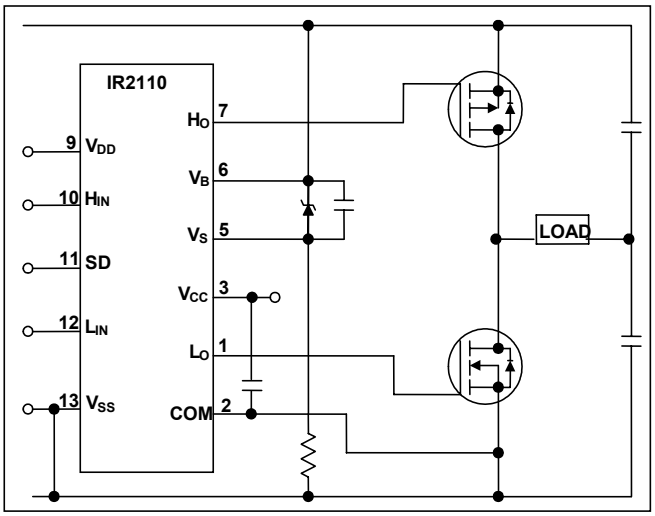


Figure 31: IRS2110 Driving a High-Side P-Channel

16. TROUBLESHOOTING GUIDELINES

To analyze the waveforms of the floating channel of the IR2110 a differential input oscilloscope is required. It is assumed that any voltage differential not referenced to ground is measured in this way.

It is also assumed that obvious checks have been made, for example:

- Pins are correctly connected and power supplies are decoupled.
- The bootstrap charging diode is ultra-fast, rated for the rail voltage.
- The shutdown pin is disabled.
- Logic inputs do not cause simultaneous conduction of devices, unless the topology requires it.

SYMPTOM	POSSIBLE CAUSE
No gate drive pulses	Verify that V_{CC} is above the UV lockout value
Gate drive pulses on lower channel only	Measure voltage across bootstrap capacitor; it should be above the lockout level. If it is not, check why capacitor doesn't get charged. Insure that capacitor is charged at turn-on.
Erratic operation of top channel	• Verify that V_S doesn't go below COM by more than 5-10 V • Verify that high side channel does not go in UV lockout • Verify that dv/dt on VS with respect to COM does not exceed 50V/ns. If so, switching may need slowing down • Verify that logic inputs are noise-free with respect to V_{SS} • Verify that input logic signals are longer than 50 ns
Excessive ringing on gate drive signal	Reduce inductance of gate drive loop. Use twisted wires, shorten length. If reduction of loop inductance does not bring ringing to acceptable level, add gate resistors.

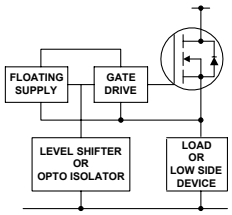
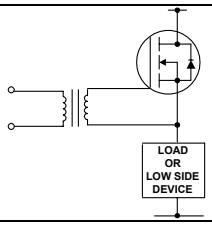
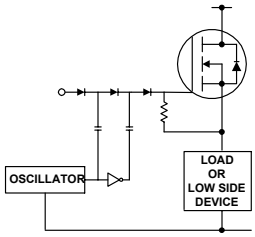
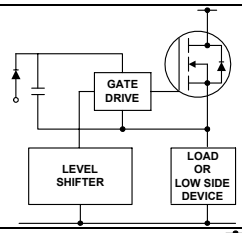
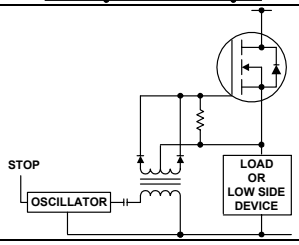
Table I		
Method	**Basic Circuit**	**Key Features**
Floating Gate Drive Supply		• Full gate control for indefinite periods of time • Cost impact of isolated supply is significant (one required for each high side MOSFET) • Level shifting a ground referenced signal can be tricky. Level shifter must sustain full voltage, switch first with minimal propagation delays and lower power consumption • Opto isolators tend to be relatively expensive, limited in bandwidth and noise sensitive
Pulse Transformer		• Simple and cost effective but limited in may respects • Operation over wide duty cycles requires complex techniques • Transformer size increases significantly as frequency decreases • Significant parasitics create less than ideal operation with fast switching waveforms
Charge Pump		• Can be used to generate an “over-rail” voltage controlled by a level shifter or to “pump” the gate when MOSFET is turned on • In the first case the problems of a level shifter have to be tackled • In the second case turn on times tend to be too long for switching applications • In either case, gate can be kept on for an indefinite period of time • In efficiencies in the voltage multiplication circuit may require more than two stages of pumping
Bootstrap		• Simple and inexpensive with some of the limitations of the pulse transformer: duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor • If the capacitor is charged from a high voltage rail, power dissipation can be significant • Requires level shifter with its associated difficulties
Carrier Drive		• Gives full gate control for an indefinite period of time but is somewhat limited in switching performance. This can be improved with added complexity

Table II			
	Die Size	**Rise Time**	**Fall Time**
	HEX-2	2.5 ns	17 ns
Typical switching times for different HEXFET die sizes	HEX-3	38 ns	23 ns
	HEX-4	53 ns	34 ns
(V_{CC}=15 V, test circuit as in Figure 9, without gate network)	HEX-5	78 ns	54 ns
	HEX-6	116 ns	74 ns

References:

1. "New High Voltage Bridge Driver Simplifies PWM Inverter Design," by D. Grant, B. Pelly. PCIM Conference 1989

2. Application Note AN-967 "PWM Motor Drive with HEXFET III" **see http://www.irf.com/technical-info/appnotes/an-967.pdf**

3. Application Note AN-961 "Using HEXSense in Current-Mode Control Power **see http://www.irf.com/technical-info/appnotes/an-961.pdf**

4. Application Note AN-959 "An Introduction to the HEXSense" **- see http://www.irf.com/technical-info/appnotes/an-959.pdf**

5. "Dynamic Performance of Current Sensing Power MOSFETs" by D. Grant and R. Pearce, Electronic Letters, Vol. 24 No. 18, Sept 1, 1988