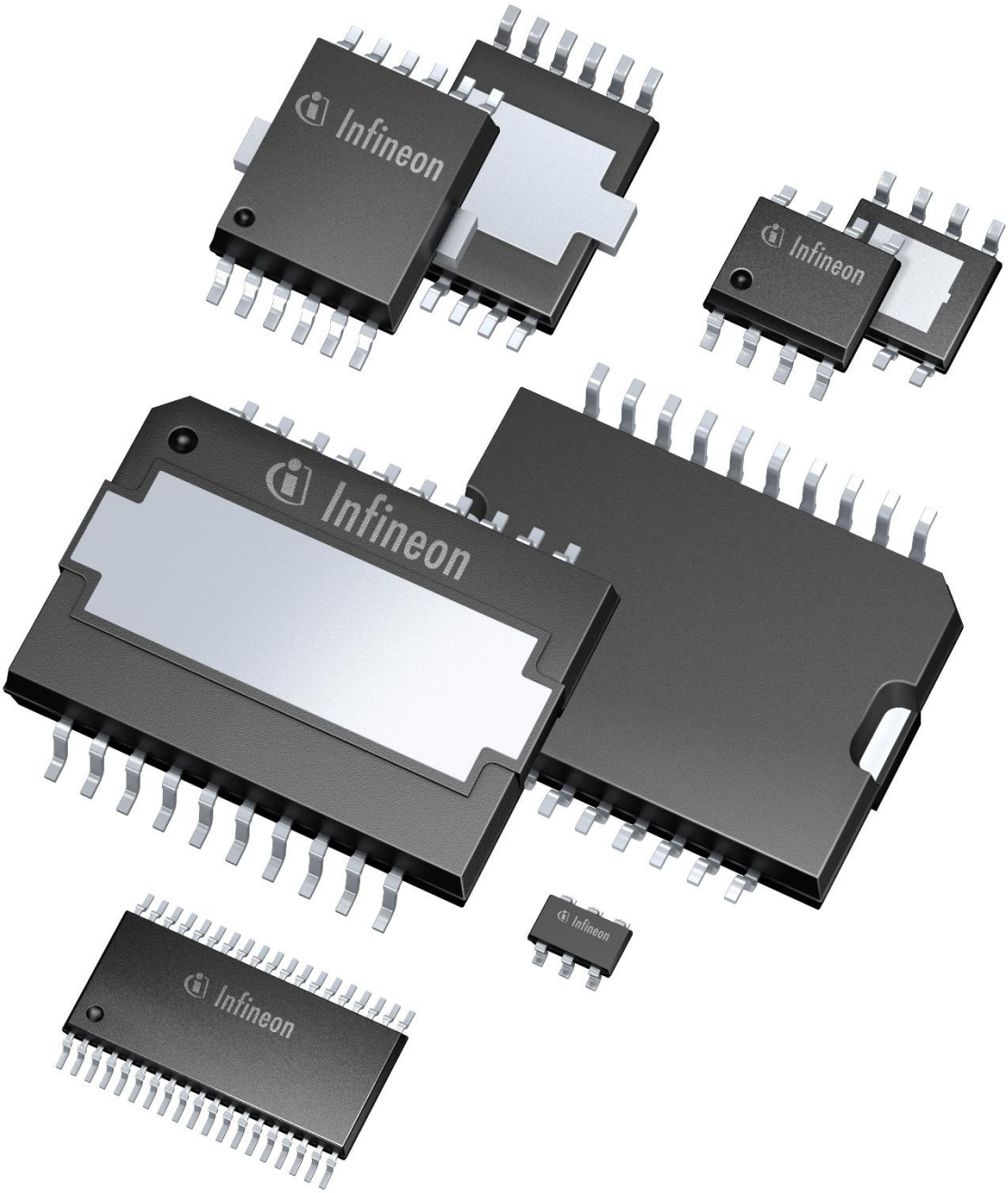
Recommendations for Board Assembly of Infineon Packages with Dual Row Gullwing Leads



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Acronyms and Abbreviations

AOI	Automated Optical Inspection
AXI	Automated X-ray Inspection
Sn	Tin plating
DDPAK	Double Discrete Package
DSO	Dual Small Outline package
ESD	Electrostatic Discharge
HDSOP	Heatspreader Dual Small Outline Package
IC	Integrated Circuit
MSL	Moisture-Sensitivity Level
Ni/Pd/Au	Nickel/Palladium/Gold plating stack-up
NSMD	Non-Solder Mask Defined pad
PG	Plastic Green
PCB	Printed Circuit Board
PPF	Pre-Plated lead Frame
QDPAK	Quadruple Discrete Package
QFP	Quad-Flat Package
SAC	Tin Silver Copper (SnAgCu) based solder alloy
SC	Semiconductor package
SCT	Semiconductor Transistor package
SMD	Solder Mask Defined pad
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
SOD	Small Outline Diode
SOP	Small Outline Package
SOIC	Small Outline Integrated Circuit package
SOT	Small Outline Transistor
SSOP	Shrink Small Outline Package
TDSO	Thin Dual Small Outline package
TOLT	Transistor Outline Leadless Top-side cooling
TSC	Top-Side Cooling
TSDSO	Thin Shrink Dual Small Outline package

Acronyms and Abbreviations

TSOP	Thin Small Outline Package
TSSOP	Thin Shrink Small Outline Package

1 Package Description

This recommendation provides information about the board assembly of Infineon lead frame based packages with gullwing lead form that are assembled by Surface Mount Technology (SMT). The leads are bent outwards from the package mold body side forming a distinct “foot” and “heel” geometry that is soldered to the Printed Circuit Board (PCB) pad. Such formed leads result in a stand-off distance between the gullwing foot landing area and the exposed die pad plane which normally has a value of 100 µm.

This document does not discuss Quad-Flat Packages (QFP) with leads on four sides of the package mold body. These package families are described in a separate document.

1.1 Dual Row SO Package Type

Infineon Small Outline (SO) or Small Outline Integrated Circuit (SOIC) packages feature gullwing shaped leads protruding mostly from the two long sides of the package mold body. SO package variants with exposed pad or heat slug provide optimized thermal performance for high density Integrated Circuit (IC) solutions.

Dual Small Outline (DSO) packages are dual row SO packages with lead pitch of 1.27 mm to 0.65 mm while certain families can also feature pitches of 1.0 mm and 0.5 mm. Due to their various devices, the DSO packages comprises most diverse configurations when it comes to e.g. die pads and heat slugs.

The DSO family can broadly be classified by their mold body width of 150 mil (e.g. DSO-8 or DSO-16), 300 mil (e.g. DSO-24, DSO-28) or 430 mil (e.g. DSO-20, DSO-36). The Thin (TDSO) and Thin Shrink DSO (TSDSO) packages feature a decreased component height and an increased integration level. **Figure 1** shows representatives of the DSO package families.

- PG-DSO packages
- PG-TDSO packages
- PG-TSDSO packages

PG = Plastic Green
T = Thin
S = Shrink
DSO = Dual Small Outline

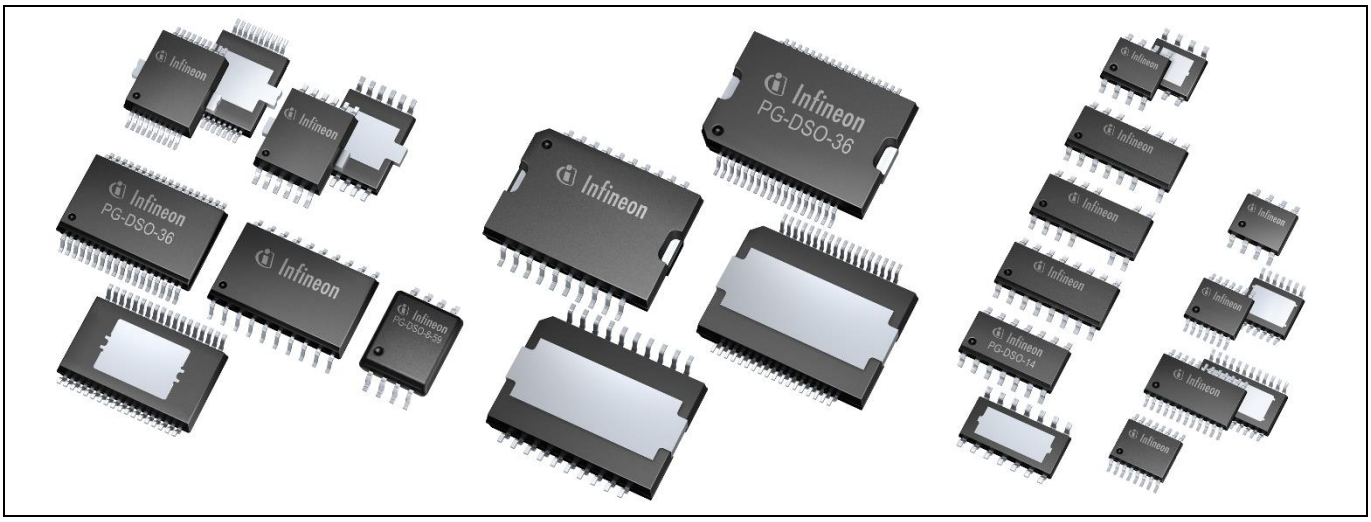

Figure 1 Examples of DSO packages.

Package Description

The Small Outline Package (SOP) families comprise dual-inline packages with smaller form factors and typical lead pitch of 0.65 mm to 0.5 mm. **Figure 2** shows examples of SOP type packages.

- PG-TSOP
- PG-TSSOP
- PG-SSOP

PG = Plastic Green
T = Thin
S = Shrink
SOP = Small Outline Package

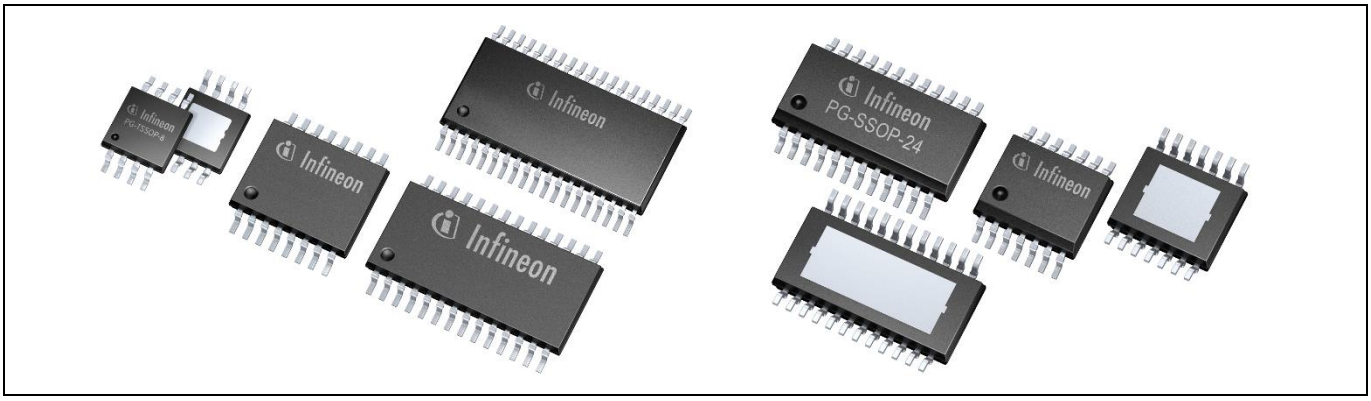

Figure 2 Examples of SOP packages.

1.2 Diode and Transistor Package Type

Semiconductor (SC) packages are near-chip-scale components with single or multiple devices. Depending on their integration level and device type, the Small Outline Diode (SOD), Transistor (SOT), SC Transistor (SCT) or Thin Small Outline Packages (TSOP6) can feature symmetric or non-symmetric pinout configuration with a maximum pin count of up to 6. **Figure 3** shows examples of SC, SCT, SOD, SOT and TSOP6 type packages.

- PG-SC59,74 packages
- PG-SCT595 packages
- PG-SOD323
- PG-SOT23, 143, 223, 323, 343, 363 packages
- PG-TSOP6

PG = Plastic Green
SC = Semiconductor
SCT = Semiconductor Transistor
SOD = Small Outline Diode
SOT = Small Outline Transistor
TSOP = Thin Small Outline Package

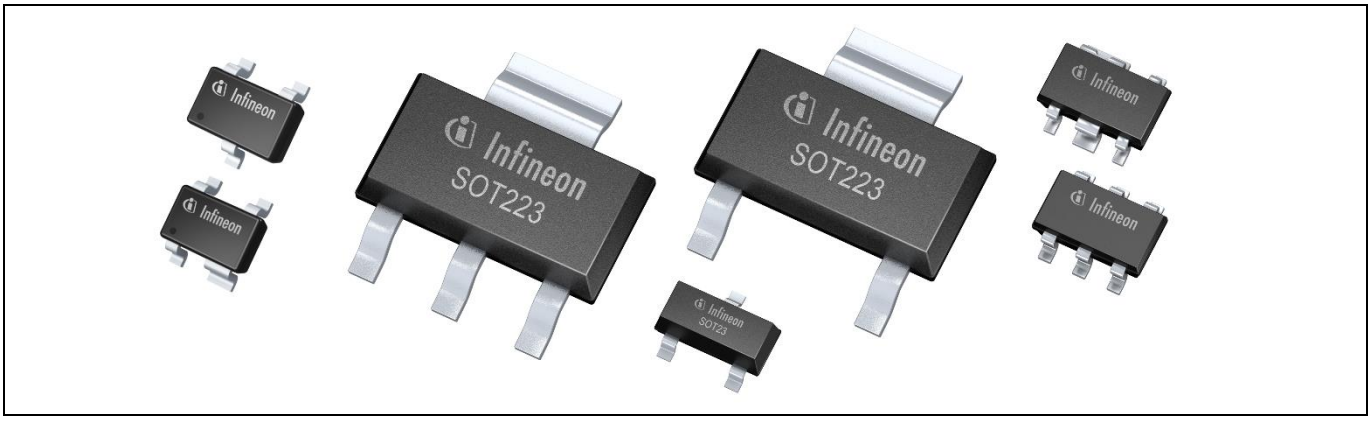

Figure 3 Examples of diode and transistor packages.

1.3 Top-Side Cooling Package Type

The Top-Side Cooling (TSC) concept allows for decoupling the thermal management from the PCB pad design. Therefore, the heat slug is situated at the top of the package. The Infineon TSC package family with gullwing leads comprises Heatspreader Dual Small Outline Packages (HDSOP) such as the Transistor Outline Leadless Top-side cooling package (TOLT), the Quadruple Discrete Package (QDPAK) or the Double Discrete Package (DDPAK). The Dual Small Outline (DSO) package family provides TSC components as well. **Figure 4** shows examples of TSC DSO and HDSOP type packages.

- PG-DSO packages
- PG-HDSOP

PG = Plastic Green
DSO = Dual Small Outline
H = Heatspreader
DSOP = Dual Small Outline Package

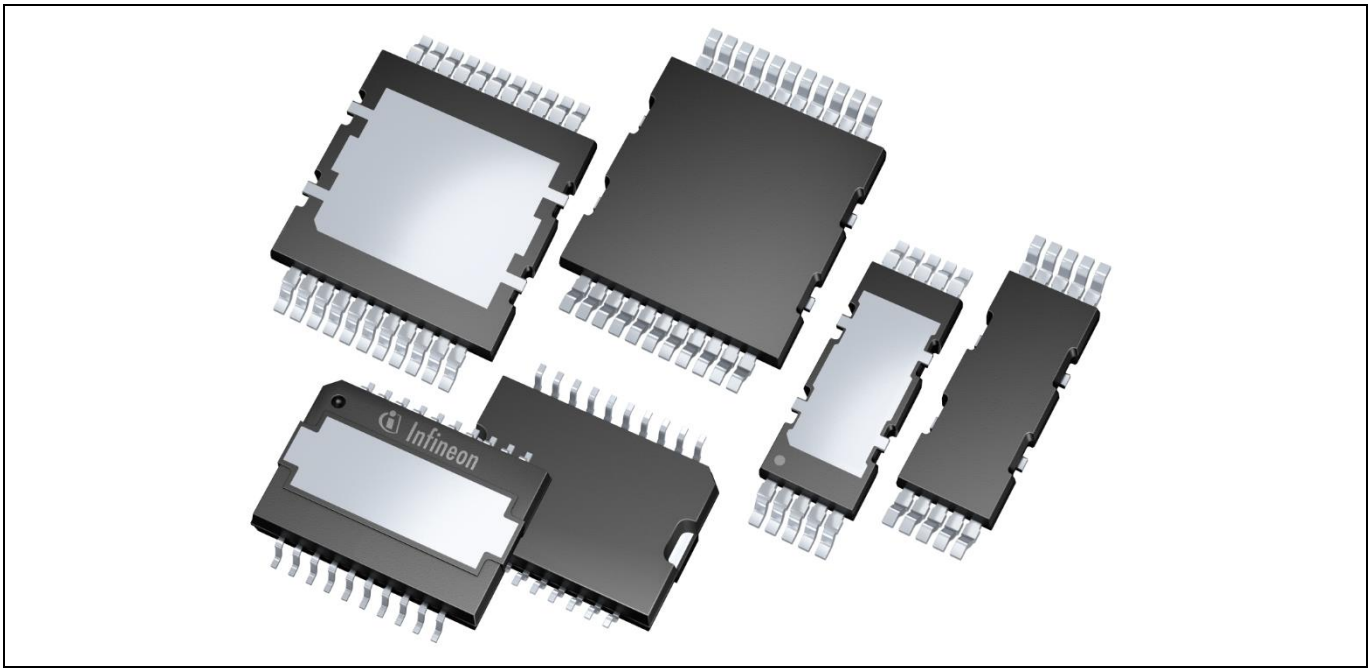

Figure 4 Examples of top-side cooling packages.

For information about the optimal thermal management and assembly considerations such as top-side heatsink mounting , please review the product-specific application notes or contact your local Infineon sales, application, or quality engineer.

1.5 Package Features and General Handling Guidelines

The SO and SC package families cover a large variety of applications including power and non-power versions with different size, thickness, pin count and thermal management.

General Handling Guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), certain moisture levels, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

For further information about component handling, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Internal Construction

Infineon packages with gullwing leads are available in non-exposed pad and exposed pad configuration. Non-exposed pad versions have the mold compound covering the entire die paddle as can be seen in **Figure 5**. In components with exposed pad the center lead frame area is exposed to the bottom side of the package. The exposed pads can be soldered to the Printed Circuit Board (PCB) for mechanical, electrical and thermal connection. DSO packages can also feature heavy heat slugs with further improved thermal performance (see **Figure 6**). Multi die pad solutions are also possible depending on the application.

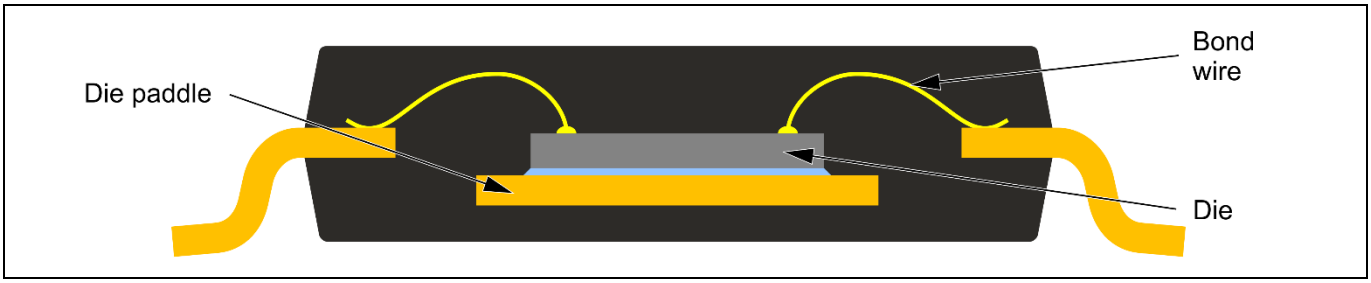

Figure 5 Schematic showing the inner setup of a gullwing leaded package without exposed pad.

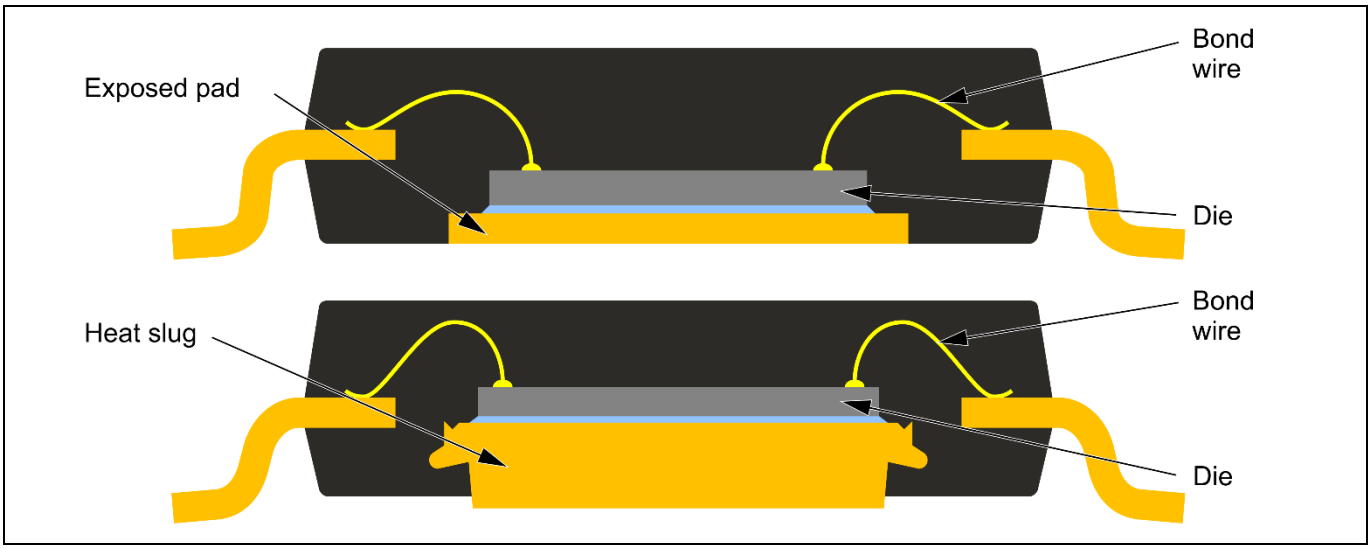

Figure 6 Schematics showing the inner setup of gullwing leaded packages with exposed pad (top) and with heat slug (bottom).

Package Description

TSC components are usually manufactured by reverse lead bending method resulting in the die being mounted on the lead frame in flipped position (see **Figure 7**).

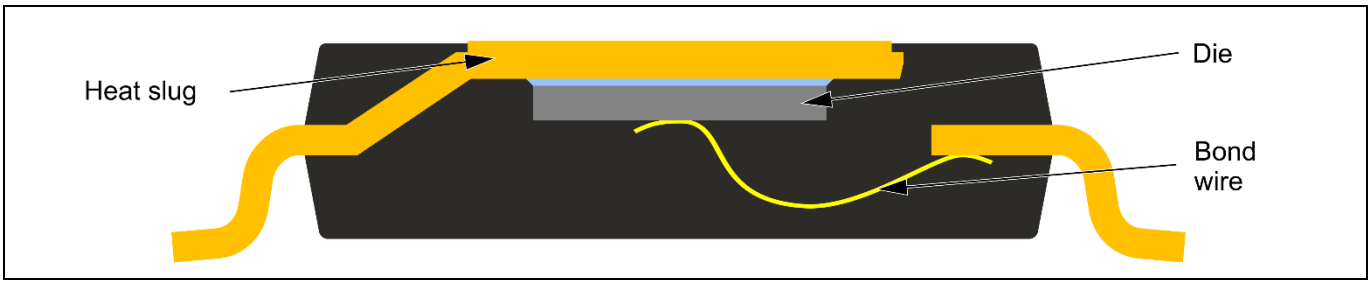

Figure 7 Schematic showing the inner setup of a top-side cooling package with positive stand-off.

Termination Design

To form gullwing-shape terminations, the leads are bent outwards at the tip. These bent lead foot and heel areas form the seating plane which is soldered to the PCB. Generally, the gullwing lead is considered one of the most reliable terminations for SMD. There are different variations available with respect to their aspect ratio or bending radius. The specific geometry depends on the application and cannot necessarily be deduced by e.g. the termination pitch or the mold body size. In **Figure 8** examples of different gullwing lead geometries are shown. They are roughly arranged by their aspect ratio and the lead frame thickness.

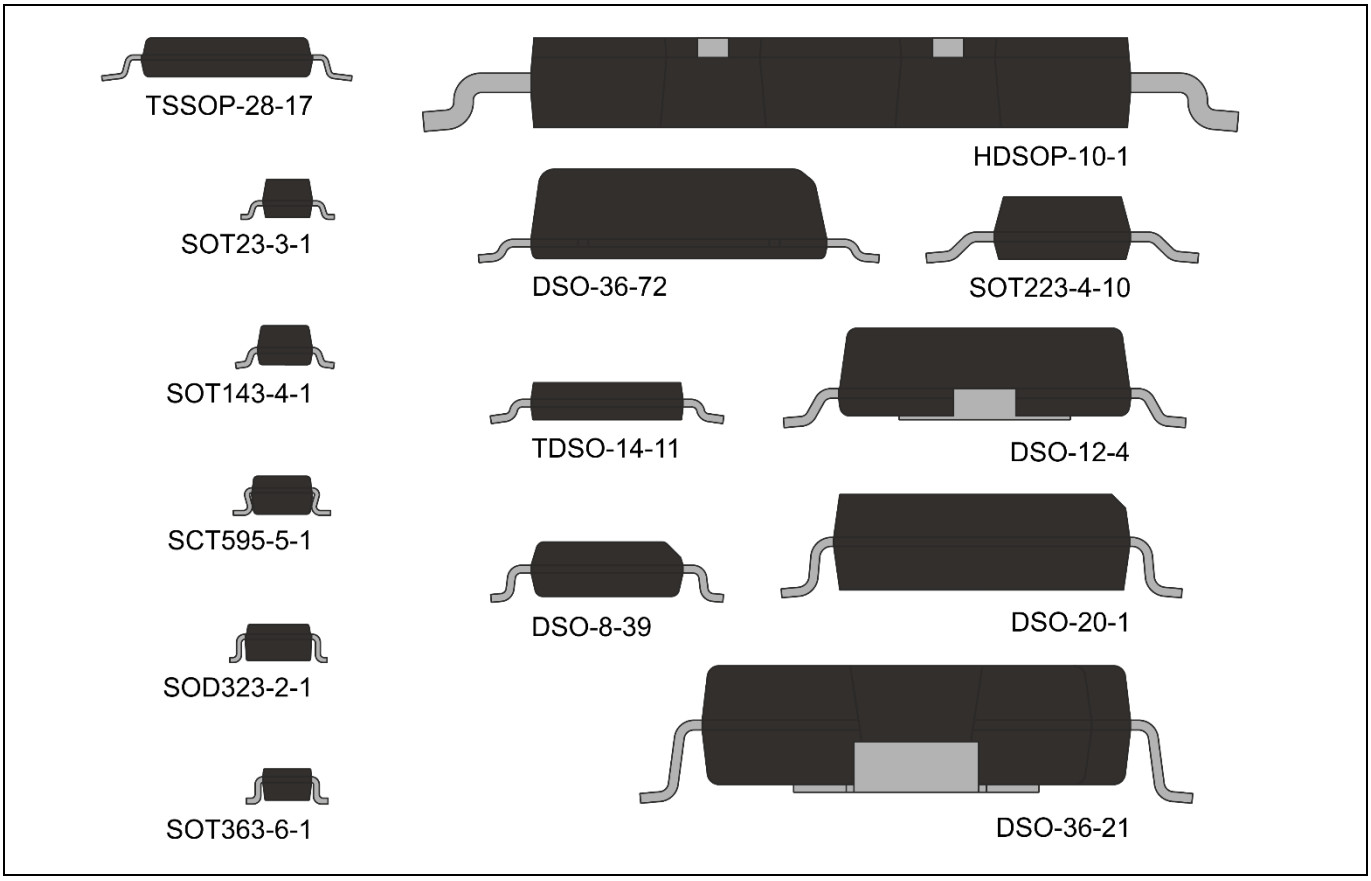

Figure 8 Examples of different gullwing lead geometries and thicknesses.

For further information about the specific component configuration, please contact your local Infineon sales, application, or quality engineer.

Termination Plating

Most of the Infineon packages with gullwing leads feature a tin (Sn) surface finish that is applied to the base metal by a post-mold process. The Pre-Plated lead Frame (PPF) provides an alternative solderable surface that is already deposited on the lead frame prior to the die attach process. The PPF surfaces basically consist of a nickel/palladium/gold (Ni/Pd/Au) stack-up. While the Sn melts during reflow, the sacrificial Au/Pd layer of the PPF surface is dissolved. The solder connection is then made to the Ni layer.

Figure 9 shows cross-sections of gullwing leads with Sn plated and PPF surface. Although the appearance of solder wetted PPF surfaces is slightly different to Sn surfaces it is in full agreement with IPC-A-610 standard [6]. Images of the outer solder joint appearance can be found in **Figure 16**.

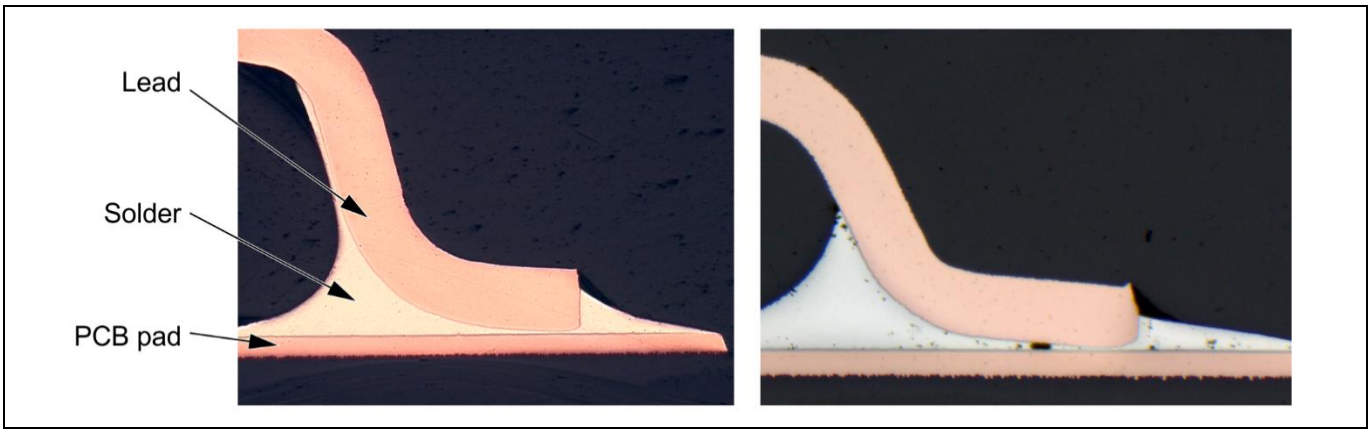

Figure 9 Soldered gullwing lead with post-mold plated Sn (left) and with pre-plated Ni/Pd/Au (right).

2 Printed Circuit Board

2.1 Routing

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite one another on either side of a PCB if double-sided mounting is used. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, the board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 Pad Design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (Solder-Mask Defined, SMD or Non-Solder-Mask Defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

The NSMD pad design is recommended for DSO, SOP as well as diode and transistor packages with gullwing leads. The approach applies to the peripheral terminations as well as to the exposed pads. Mixing different pad definition types in one footprint is not recommended.

Beside their electrical function, the exposed pad or heat slug areas of SO packages are designed to conduct high thermal loads into the PCB in order to achieve an optimal thermal performance. Therefore, the exposed pad area on the PCB should be at least congruent with the area on the package. Using a PCB pad of the same size as the package exposed pad will also increase the solder joint reliability, and the electrical performance for some applications. **Figure 10** shows different approaches of print pattern on a PCB pad for a package heat slug connection.

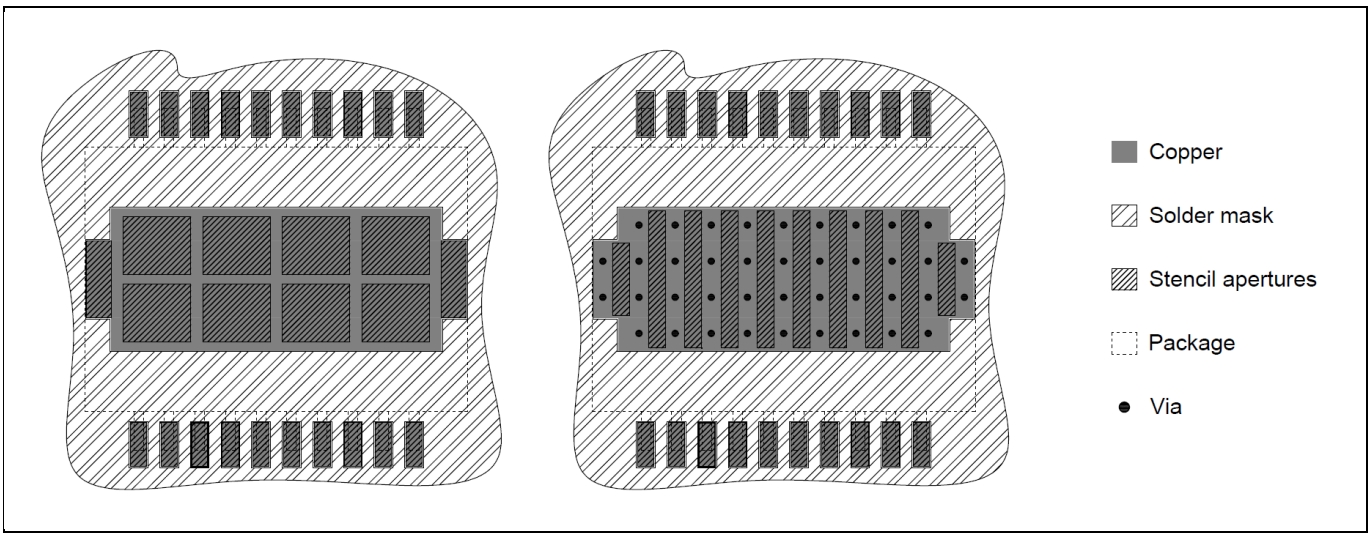

Figure 10 Examples of DSO-20 footprints without (left) and with via-in-pad design (right).

Figure 11 shows schematic depictions of a backward PCB pad extension for gullwing leads which is necessary for an optimal solder fillet formation in the lead heel. According to the IPC-A-610 the minimum solder wetting height shall reach an extended line projected from the lead tip top corner in parallel to the PCB pad plane [6].

As a rule of thumb often the line parallel to the lead top plane is used to take into account the lower bend angle.

The PCB pad and therefore the solder paste print should have a distinct distance to the package mold in order to avoid an unclean solder process as it is induced by e.g. solder spatters.

Generally, an optimal PCB design depends on the specific application as well as on the specific design rules of the chosen board manufacturer.

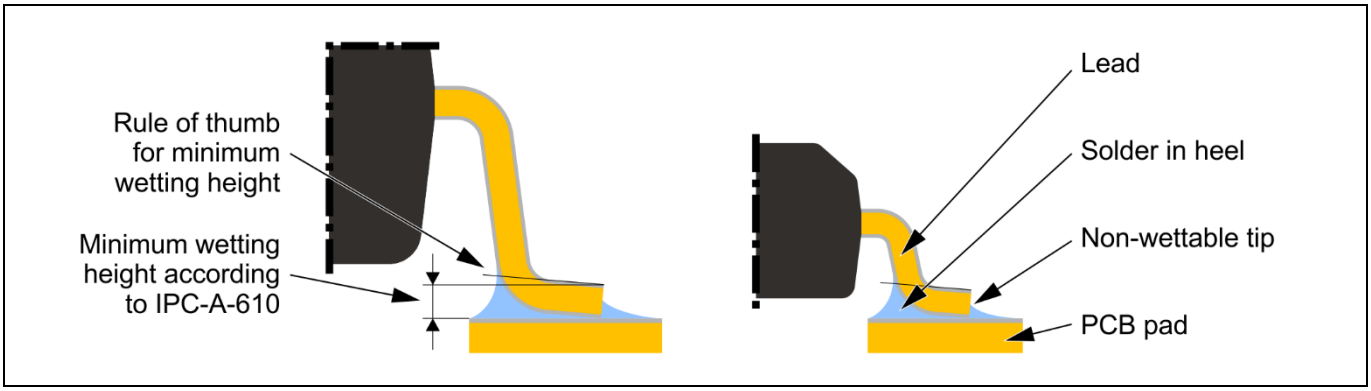

Figure 11 Schematic depictions of the backward PCB pad extension for optimal solder fillet formation in heel according to a rule of thumb and to the IPC-A-610 [6].

TSC Components with Negative Stand-Off

The majority of the TSC gullwing components feature a positive stand-off between the package mold body and the landing area of the leads. The TOLT package (Infineon nomenclature: PG-HDSOP-16-1) features a negative stand-off, so that the package body is in direct contact with the PCB copper layer. **Figure 12** shows how a “dummy” copper pad on the PCB should be arranged to provide the intended mechanical support to the package. Such a pad has no thermal or electrical function.

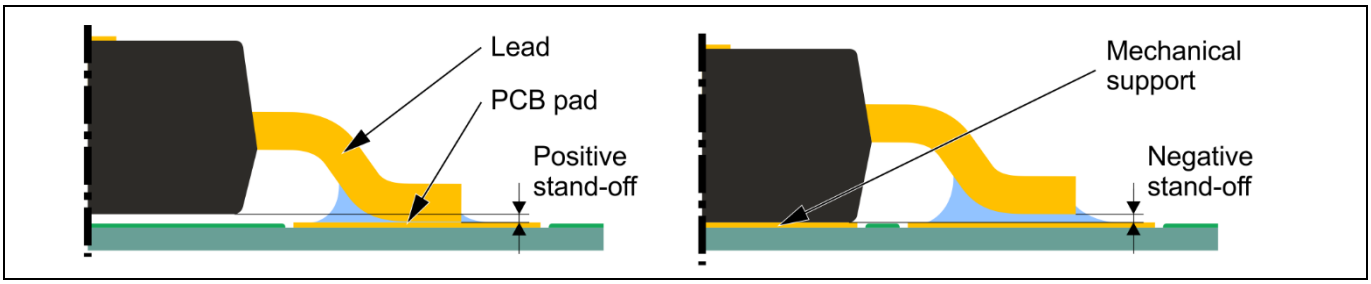

Figure 12 Top-side cooled packages with standard positive stand-off (left) and with negative stand-off (right) such as the HDSOP-16-1 (TOLT). The pseudo-pad below the package body is beneficial as a mechanical support of well-defined height.

Besides the mechanical arrangement, the solder paste print must be considered specifically as well. In order to overcome the gap that is formed by the negative stand-off, a sufficiently high amount of solder must be provided to the assembly. Internal investigations have shown, that with a stencil thickness of 200 µm and a nominal print-to-print distance of 300 µm, the assembly is prone to flux bridges after package placement. Although no solder bridges have been discovered after reflow, it is recommended to provide the necessary solder volume by extending the print to the lead tip while increasing the print-to-print distance to 400 µm. **Figure 13** shows the approach to the right in comparison with a more conservative one to the left.

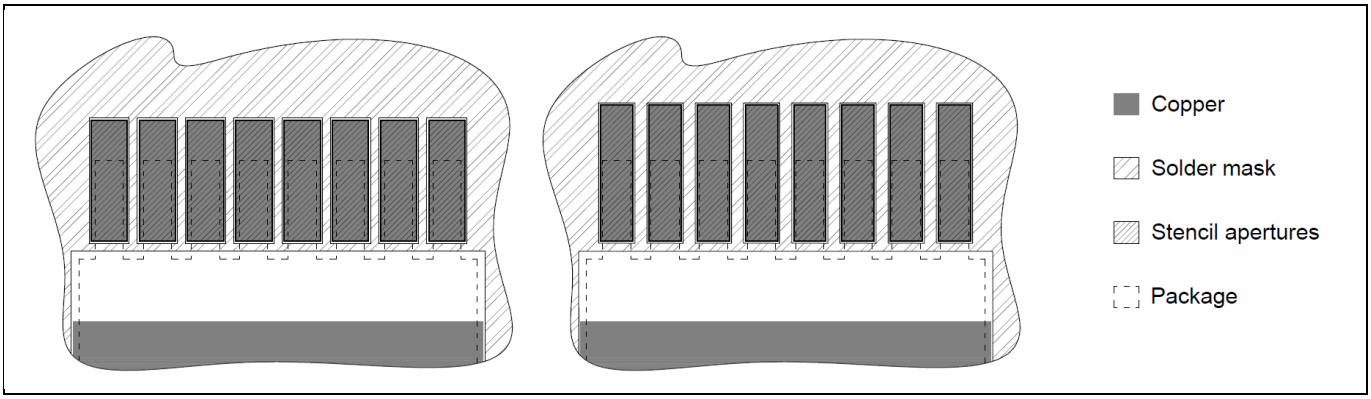

Figure 13 Footprint and stencil variations for top-side cooled HDSOP-16-1 (TOLT) package with negative stand-off. Both variants provide the same amount of solder that is necessary for proper solder fillet formation. The right design is preferred due to the elimination of flux bridges after component placement.

Information about the optimal thermal management and assembly considerations such as top-side heatsink mounting can be found in product-specific application notes.

For further information about PCB pad design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1].

Further details and specific footprint recommendations can be found in Infineon package data that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show you an example of the stencil aperture layout for each package.

Please also feel free to contact your local sales, application, or quality engineer.

2.3 Via-in-Pad Design

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-hole vias in the board. The heat is then transferred from the chip over the package die pad and the solder joint to the thermal pad on the board and further through the PCB by the thermal vias.

The diameter and the number of vias in the thermal pad depend on the specific thermal requirements of the final product, the power consumption of the product, the application, and the construction of the PCB. A typical hole diameter for thermal vias is 0.2 - 0.5 mm. An array with 1.0 - 1.2 mm pitch can be a reasonable starting point for further design optimization. The implementation of thermal vias has several impacts on the board assembly as outlined below. A constant increase of number of vias does not necessarily translate into a constant decrease of the thermal resistance of the entire assembly set-up. Thermal and electrical analysis and/or testing together with a proper board assembly design procedure are recommended to determine the optimal number of vias needed.

One of the primary exposed pad design objectives, besides the thermal management, should be to avoid the penetration of the vias by solder. Consequences of such solder wicking can be a decreased stand-off between the PCB and the package, an increased void formation ultimately resulting in an insufficient solder joint area, or surplus solder on the opposite side of the PCB.

A first approach for risk reduction should be the prevention of a direct print of solder paste on the via orifice. Since the stencil for large area prints such as on die pads is usually segmented, it is a good practice to position the vias under the stencil sheet beams as shown in **Figure 10**. With such an approach, a good solder joint on a central die pad can be formed using vias that remain open on both sides of the board.

Despite the precautionary stencil design approach, the solder can move into the via, driven by the wetting forces. If the solder then protrudes to the opposite side of the PCB, it may interfere with a second solder paste print process. To minimize the effect, dummy areas on the opposite side as shown in **Figure 14** can catch the surplus solder to avoid beading and solder lumping.

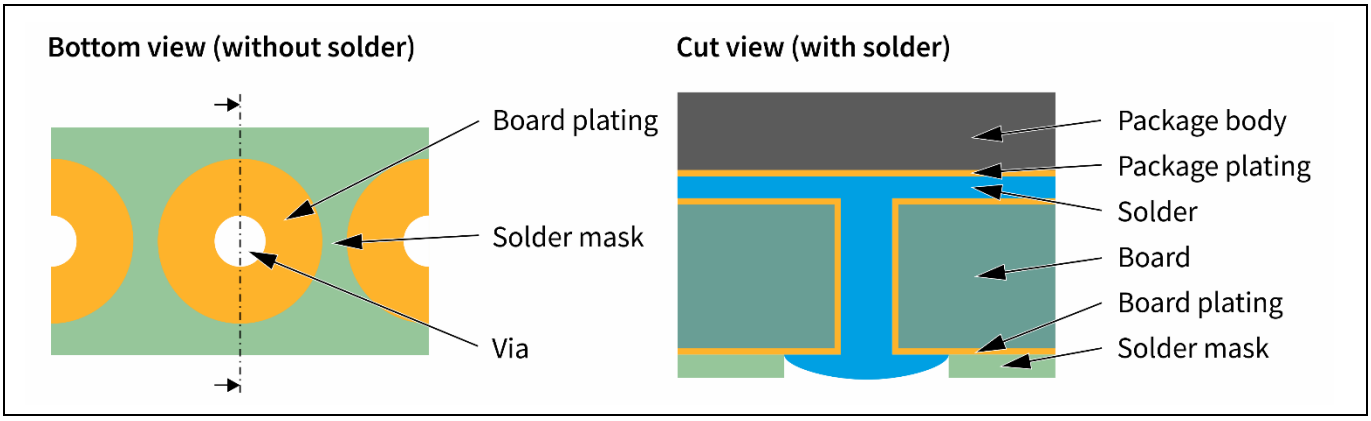

Figure 14 Wettable “dummy” area on the opposite side of the board surrounds the vias to act as a buffer for surplus solder.

In case the solder variance in volume below the die pad is too high due to the wetting of vias, they can be closed by “tenting.” This process includes covering the vias by a solder mask (e.g. dry-film solder mask). If the via tenting is done only on the opposite side of the board, the voiding rate will increase significantly. Another method to close vias is called “plugging” (filling with epoxy), followed by overplating. Very small vias (100 µm in diameter or smaller) should be filled with copper and overplated. In both cases, the specification of a planar filling is necessary to avoid cavities that will trap gases, forming voids during reflow soldering.

In case it is not necessary to provide a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias can be placed next to the footprint near the package and covered with solder mask.

For further information about vias in pad, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB Assembly

3.1 Solder Paste Stencil

In SMT the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut stencils (mostly made from stainless steel) are preferred.

The stencil apertures are usually of the same dimensions as the relevant pad on the PCB. In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. For typical DSO and SOP packages, stencils 120 µm to 150 µm thick are recommended. For the smaller diode and transistor packages choosing a stencil of 100 µm thickness can be reasonable. HDSOP components with top side cooling can even be in need of up to 200 µm stencil thickness especially when there is an increased lead-to-pad gap caused by a negative stand-off. Extending the solder pads together with the print can provide such an increased solder volume as shown in **Figure 13**.

The solder paste volume in apertures larger than approximately 5 mm may be scooped out depending on the specific squeegee pressure and rigidity. Such apertures necessary for many die pad prints, should be segmented into smaller areas. When reducing the die pad print the stand-off between gullwing landing area and die pad plane has to be considered. Normally, this distance is of 100 µm. Therefore, the reduction is with approx. 70% lower compared with leadless packages, where pins and pads are in one plane. When choosing the print pattern and reduction, also the volume and height, provided by the solder stencil thickness has to be considered. Areas on the pad, which are not covered by print, are preferred positions for vias as shown in **Figure 10**.

For individual design adaptations to reach the optimal amount of solder, the stencil thickness, the PCB pad finish, solder mask quality, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder Paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. Using Type 3 or Type 4 paste is recommended for the assembly of packages with gullwing leads, depending on the specific stencil aperture size and therefore solder paste transfer efficiency.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides on the surface.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects

the potential need for removing the flux residuals after the assembly. For SMD packages where the solder joint is mainly formed on the package bottom side, a “no clean” paste is recommended to avoid subsequent cleaning steps underneath the package. Small gaps make cleaning highly difficult if not impossible. Certain precautions have to be taken if any kinds of flux residues remain on the board prior to any kind of coating. For power packages, leakage currents and the potential for shorting below components have to be considered when choosing the specific flux type (e.g. halide-free vs. zero halides).

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended, especially for packages with small termination and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately prior to the mounting process.

For further information about component placement, please refer to *the General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow Soldering

For PCB assembly of gullwing packages, the widely used method of reflow soldering in a forced convection oven is recommended. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Power packages where leakage currents and shorting below the component have to be considered should be soldered with decreased flux spreading. Therefore, it is recommended to optimize the reflow profile in such a way that excessive flux or solder spattering is avoided.

Minimum Reflow Conditions

The lower temperatures and durations of an optimal reflow profile must stay above those of the solderability qualification. The solderability of the terminations of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum Reflow Conditions and Cycles

Components that are Moisture-Sensitivity Level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, including a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

PCB Assembly

Typical Infineon packages with gullwing leads are generally suited for mounting on double-sided PCBs. However, top-side cooled packages should not run bottom-up through a second reflow cycle in order not to alter stand-off dimensions for later heat dissipator mounting. Solder joints of components on the first PCB side will again reflow in the second step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held in place by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity will force the components closer to the PCB surface. This shape will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

For further information about reflow soldering, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a component is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Inspection

5.1 Optical Solder Joint Inspection

Irrespective of the specific geometry of a gullwing lead the solder joint is generally considered to be of good quality when the heel region is wetted up to a certain height and additionally the sidewall is sufficiently covered by solder. **Figure 15** shows optical side-views of two properly soldered packages with gullwing leads of different geometries. The tips of the gullwing leads have bare copper (e.g. cut edges) that is not intended to wet by design according to the IPC-A-610 [6].

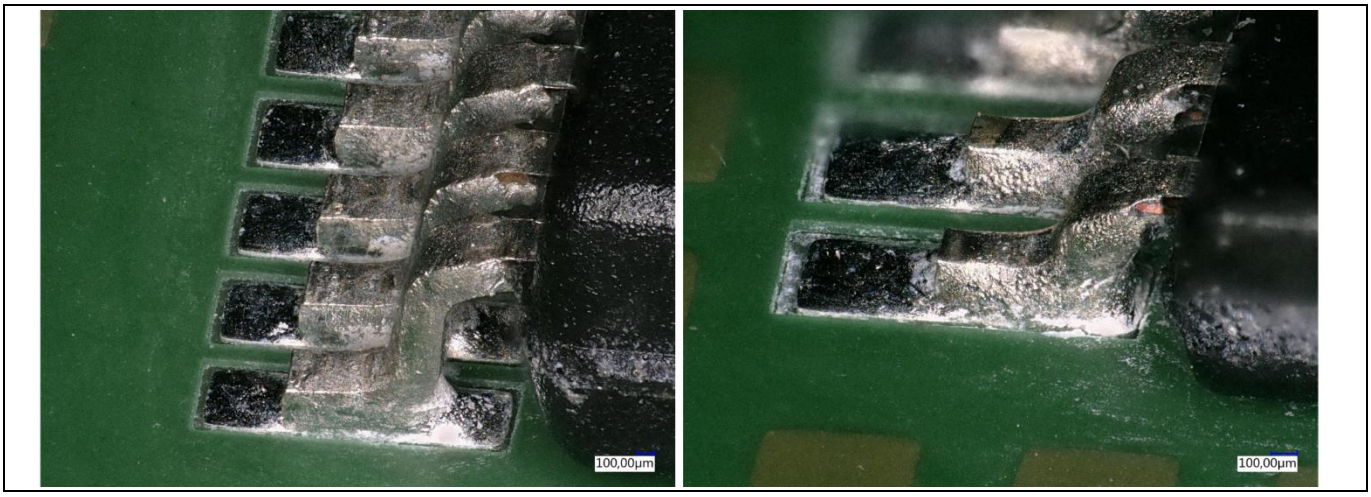

Figure 15 Examples of optical images of DSO-36 (left) and TSDSO-14 (right) gullwing leads.

The visual inspection of the solder joints of the outer, gullwing-shaped terminations with conventional Automated Optical Inspection (AOI) systems is a standard procedure. As can be seen in **Figure 16** gullwing leads with PPF surface can appear different on their top side from those with Sn plating because the plated surface does not melt together with the plating during reflow. According to IPC-A-610 the top side of a gullwing lead is not taking part in the solder joint formation [6].

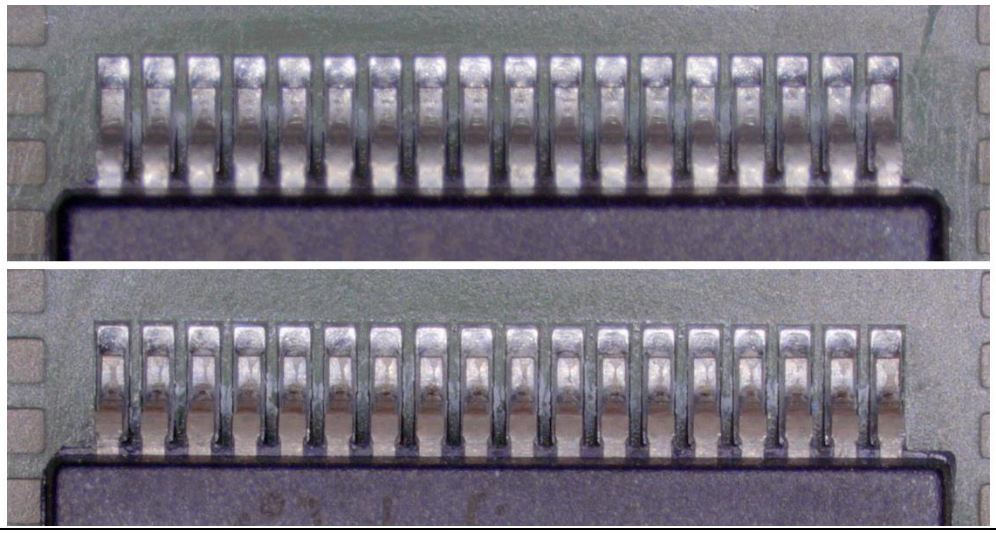

Figure 16 Top view photographs of DSO-36 gullwing leads with Sn plating (top) and with PPF surface (bottom). In the latter example, the top side of the leads does appear different because the plating does not melt together with the solder during reflow.

For engineering tasks, cross-sectioning can offer detailed information about the solder joint quality. Due to its destructive character, cross-sectioning during monitoring is naturally not practical.

For further information about the acceptability of electronic assemblies inspected optically, please also refer to the IPC-A-610 standard [6].

5.2 X-Ray Solder Joint Inspection

Automated X-ray Inspection (AXI) systems are appropriate for efficient inline control of component parts that cannot be inspected properly by optical systems (such as exposed pads). AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 17 shows typical X-ray photographs of DSO-20 and DSO-36 components. The internal lead frame, as well as wire bonds, and the solder joints that connect the package to the PCB are visible. Large exposed pads may tend to increased voiding because they do not provide a sufficient ratio between volume and surface necessary for proper outgassing of the organic paste compounds during reflow. Generally, the extent of voiding depends on the board pad size, the via and stencil layout, the solder paste, and the reflow profile. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment or the electrical use of the component.

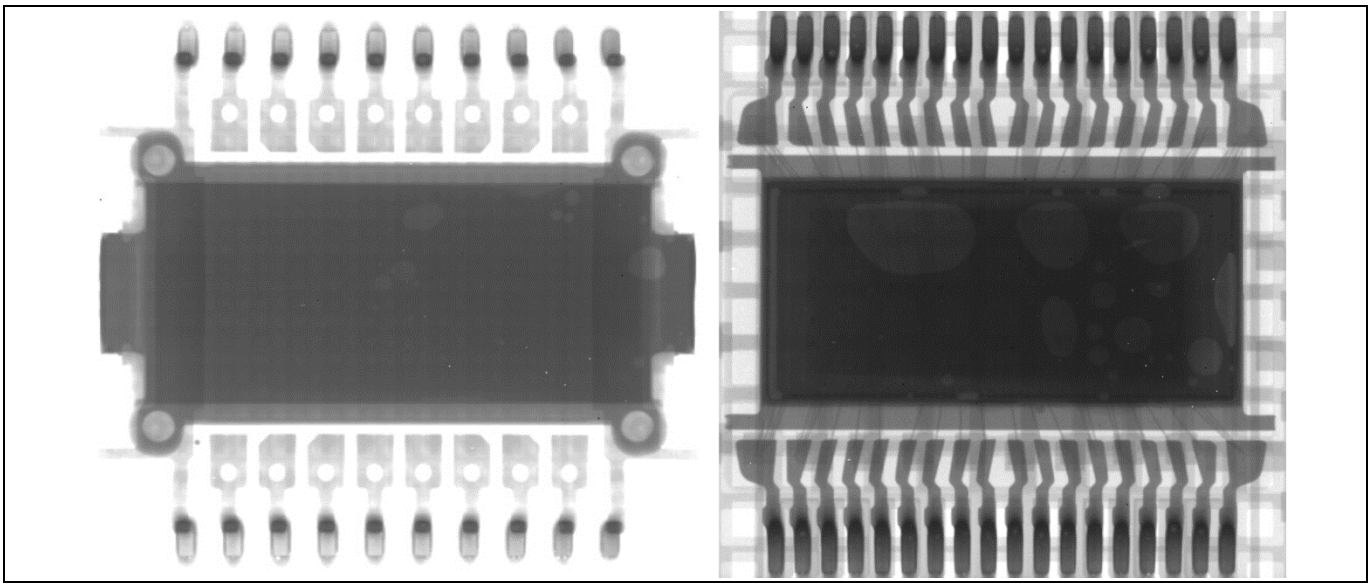

Figure 17 X-ray photographs of a properly soldered DSO-20 (left), and a DSO-36 (right) package.

6 Rework

In general, gullwing lead components are reworkable. Single solder joint repair of small pitch terminated packages can, however, be very difficult and is not recommended. The reuse of completely de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to desolder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (ie onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

7 References

[1] Infineon: Packages. www.infineon.com\packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision History

Page or reference	Major changes since the last revision
Section 6 “Rework”	Update of sample conditions in case of return.
Entire document	Editorial review.

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