

Isolated gate driving solutions

Increasing power density and robustness with isolated gate driver ICs

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About this document

Scope and purpose

This application note presents isolated gate driving solutions to increase the system efficiency, power density and robustness of high-performance power conversion applications. A comparison between the classical isolated gate driving solutions based on pulse transformers and the modern solutions employing isolated gate driver ICs or digital isolators is provided. This comparison between the different driving solutions is based on the main parameters and features: isolation level, propagation delay, parasitic leakage inductance, parasitic input-to-output capacitance, Common-Mode Transient Immunity (CMTI), component size and thickness, PCB layout flexibility, and compactness. Each solution is analyzed in depth considering its advantages and disadvantages in driving Superjunction (SJ) MOSFETs, silicon carbide (SiC) MOSFETs and gallium nitride (GaN) High-Electron-Mobility Transistors (HEMTs). EiceDRIVER™ GaN and EiceDRIVER™ **2EDi**, **1EDB**, **2EDN**, **1EDN** and **1EDN-TDI** product families are suggested for the different isolated gate driving solutions.

Intended audience

This application note is targeted at application engineers and designers of SMPS looking for isolated gate driving solutions for SJ MOSFETs, SiC MOSFETs and GaN HEMTs. A state-of-the-art analysis of the different isolated gate driving solutions is presented here with a focus on Infineon EiceDRIVER™ product families of gate driver ICs. The aim of this application note is to guide the designer in the selection of the right driving solution according to the specific needs and constraints of the application.

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1 Introduction

Galvanic isolation is a key element to be considered during the design of SMPS. The need for galvanic isolation will be briefly described, followed by the presentation of state-of-the-art isolated gate driving solutions for modern SMPS employing SJ MOSFETs, SiC MOSFETs and GaN HEMTs.

1.1 Motivation and context

Global electricity demand keeps rising year after year and at a faster pace than the overall energy demand [1]. Developing countries have been expanding their grid infrastructure to ensure that the population has access to electricity for lighting, heating and the supply of home appliances. Industrial automation and motor drives along with the electrification of vehicles, ships, trains, planes and off-grid applications are also driving the demand for more electricity. Access to fast communication infrastructure and the growth of data traffic is increasing the energy demand of telecom base stations [2]. Furthermore, the processing capacity of hyperscale data centers, cloud servers and edge computing is also expanding to support the internet traffic that keeps rising exponentially [3]. Renewables have been covering a significant share of the world's electricity generation growth, now accounting for over a quarter of global power output [1]. Solar photovoltaic (PV) inverters, hydropower and wind generators are already fulfilling the electricity demand of some countries for periods of several hours or even days. Battery Energy Storage Systems (BESS) are helping to deal with the intermittent nature of renewable sources by maintaining the balance between generation and demand in order to improve power system reliability and stabilize local issues such as voltage fluctuation.

Power electronics technologies are used for energy conversion and power management in solar PV inverters, wind generators, industrial automation, EV fast chargers and motor inverters, BESS, telecom base stations, data centers, cloud servers, home appliances and tools. Humans are involved in the operation and maintenance of these systems through Human-Machine Interfaces (HMI). The controllers and communication peripherals connected to a HMI need protection from the high-voltage circuitry of the Power Conversion System (PCS) and also from any high voltage surges that may damage the equipment or harm humans. This protection is achieved through galvanic isolation that prevents unwanted leakage currents between two parts of a system while still enabling signal and power transfer between those two parts. Furthermore, galvanic isolation improves noise immunity and prevents disruptive ground loops in systems with large Ground Potential Differences (GPDs) between primary and secondary sides of a power conversion stage. As shown in Figure 1, the galvanic isolation provided by the isolator element completely decouples the primary side from the secondary side of the system. The ground loop is interrupted, and only Differential Mode (DM) signals can pass across the isolator element, while any Common Mode (CM) noise is completely blocked. Finally, galvanic isolation is also needed to enable communication between Low-Side (LS) and High-Side (HS) components of a system, such as transferring the PWM signal from a controller (referred to as the LS ground) to drive a HS power switch of a Half-Bridge (HB) topology.

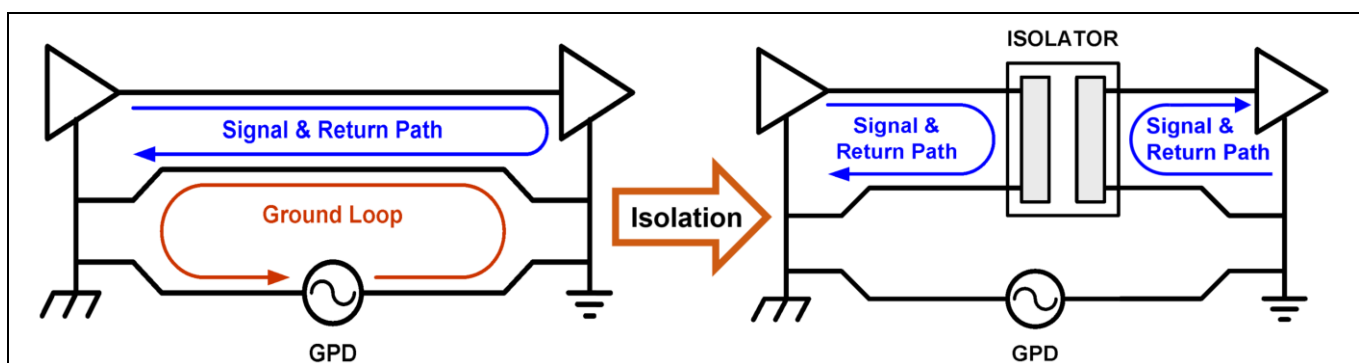


Figure 1 Galvanic isolation provided by the isolator element to interrupt the ground loop and decouple the primary side from the secondary side of the system

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1.2 Galvanic isolation in modern SMPS

Pulse transformers have been widely used to provide galvanic isolation between controller and power switches by isolating the command signals from the LS gate driver. However, besides being a bulky solution, it has other operating limitations related to the saturation of the core. By an isolator element into the gate driver, utilizing for example the Infineon's Coreless Transformer (CT) technology as shown in Figure 2, it is possible to produce functional and reinforced isolated gate driver ICs. The EiceDRIVER™ **2EDi** product family [4] is one example of these integrated gate driving solutions that can make PCB layout easier and enable high power density designs with increased robustness and timing accuracy.

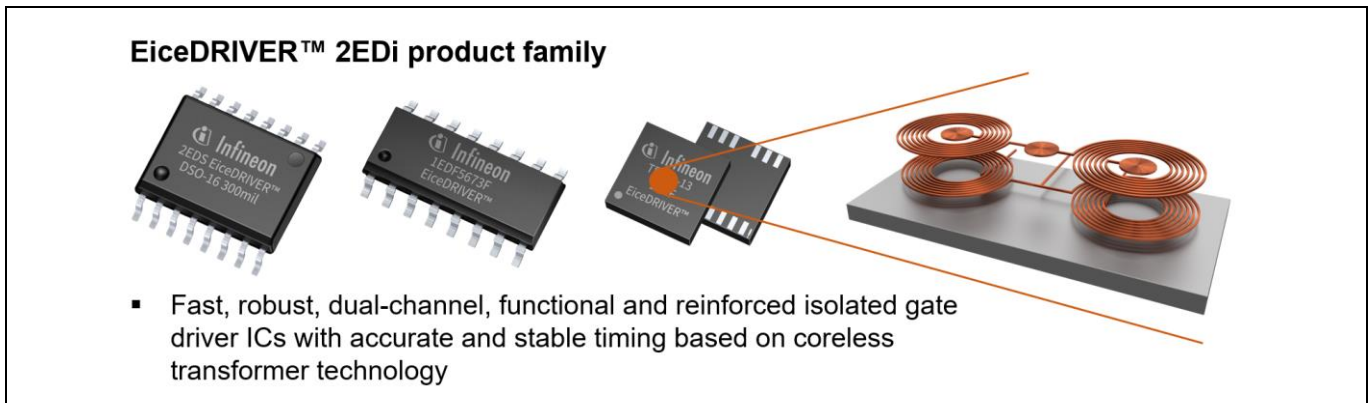


Figure 2 Coreless transformer technology enables functional and reinforced isolated gate driver ICs

The power conversion sector is always pursuing new solutions to improve efficiency, increase power density and reduce total system cost. Wide-Bandgap (WBG) semiconductors have a better on-state resistance per specific area ($R_{on} \cdot A$) than the best silicon-based technology available on the market [5]. This reduces the conduction losses and consequently enables operation at much higher temperatures. Regarding the charge stored in the output capacitance (Q_{oss}), a GaN HEMT is almost an order of magnitude better than its silicon counterpart and a factor of 2 below a SiC MOSFET [5]. These characteristics of WBG semiconductors significantly improve the switching losses and enable operation at high switching frequencies, leading to a volume reduction of the magnetic components and consequent shrinking of the PCS. However, fast switching of SiC MOSFETs and GaN HEMTs produces large di/dt and dv/dt transients that, besides the high ringing and EMI emissions, can cause spurious turn-on of the power switches due to inductive as well as capacitive feedback to the gate [6]. For that reason, it is crucial for any isolated gate driving circuit to minimize parasitic capacitances [7]. As will be discussed in section 2.1, this is a major drawback of pulse transformers that can prevent their application in isolated gate driving circuits for WBG semiconductors. The CMTI of the isolator device is also crucial to ensure that no signal corruption occurs during fast transients applied between the two separate grounds of the system. GaN HEMTs can easily generate ultra-fast slew-rate voltage transients exceeding 100 V/ns. This is why the CMTI is a key parameter to be considered during the selection of the isolated gate driving solution, especially with the advent of WBG power switches. The EiceDRIVER™ GaN product family [8] was specifically developed to ensure robust and efficient switching of the high-voltage CoolGaN™ HEMT and at the same time minimize R&D efforts and shorten time-to-market.

Figure 3 shows a typical application diagram of a SMPS using integrated galvanic isolated gate driving solutions from Infineon. The conversion stages are composed of a primary side controlled totem-pole PFC and a secondary side controlled resonant LLC converter with a Full-Bridge (FB) Synchronous Rectifier (SR).

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The grid-connected totem-pole PFC receives the PWM signals from a controller located on the same side, i.e. on the primary side of the main reinforced isolation barrier. There are no isolation requirements for safety reasons, since there is no connection with the HMI or any other communication interface located in the Extra-Low Voltage (ELV)¹ secondary side of the isolation barrier. Nevertheless, due to the input-to-output voltage requirements for the HS driver, a galvanically isolated gate driver IC can be advantageously used as an alternative to a level-shift gate driver. In this case, the isolation requirements can be more relaxed compared with the reinforced isolation standard; the IC isolation must just withstand the maximum PFC operating voltage, which is finally the stress-voltage applied between input and output side of the HS driver. This isolation requirement is referred to as “functional isolation”, since it must just guarantee the correct functionality of the HB system. In Figure 3, the functional isolated EiceDRIVER™ GaN **1EDF5673F** and the EiceDRIVER™ **2EDF7275F** are recommended to drive the CoolGaNTM power switches on the fast-switching leg and the CoolMOS™ SJ MOSFETs of the phase-rectification HB, respectively.

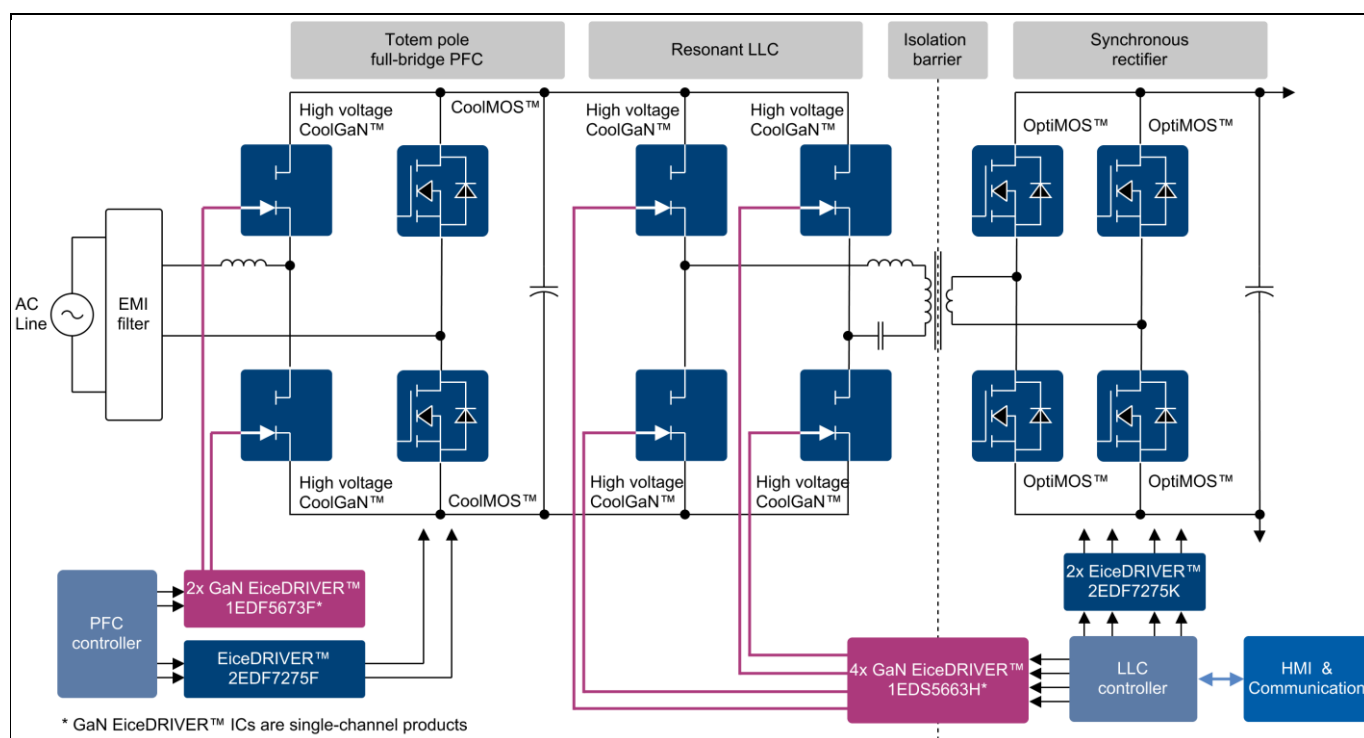


Figure 3 Typical application diagram of a SMPS using integrated galvanic isolated gate driving solutions for a primary-side controlled totem-pole PFC and a secondary-side controlled resonant LLC converter with a FB SR

The resonant LLC converter receives the PWM signals from the controller located on the secondary side. Since this controller is connected to the HMI and communication interface, reinforced isolation from the resonant LLC FB must be ensured. The first step is to create a reinforced isolation barrier on the PCB with typically 8 mm spacing between the primary and secondary side of the converter. Figure 4 illustrates the reinforced isolation barrier on a PCB of a resonant LLC converter. The second step is to use components to transmit the signals across this barrier and provide the required isolation level according to the international standards². In this

¹ ELV is an electricity supply voltage which does not exceed a nominal value of 50 V AC or 120 V DC (ripple free) at rated supply voltage between conductors or electrical conductor and earth (ground).

² An overview of safety isolation standards and certifications can be found in a previous application note [9].

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way, it is possible to guarantee that the secondary side of the SMPS is an earth-free circuit which is isolated from the AC mains supply.

The reinforced isolated gate driver ICs of the EiceDRIVER™ GaN and 2EDi families are suitable to be mounted across the isolation barrier to drive CoolGaN™ and CoolMOS™ power transistors. In case of a defect in one of the LLC MOSFETs, the gate might become a short-circuit to the drain, and the bulk voltage consequently would be applied to the gate driver IC. Since the driver IC is placed across the reinforced isolation barrier, it is of system safety relevance to ensure that the isolation inside the IC is still intact after this high-energy fault. The EiceDRIVER™ GaN **1EDS5663H** and the EiceDRIVER™ **2EDS8265H** are examples of gate driver ICs with robust input-to-output reinforced isolation ensured by the CT technology.

Since the output voltage of the SR is within the ELV range, the risk of dangerous electrical shock is limited. Then only functional isolation is required to drive the OptiMOS™ power MOSFETs. The EiceDRIVER™ **2EDF7275K** functional isolated gate driver available in the small LGA-13 package is recommended to drive the OptiMOS™ power switches of the SR.

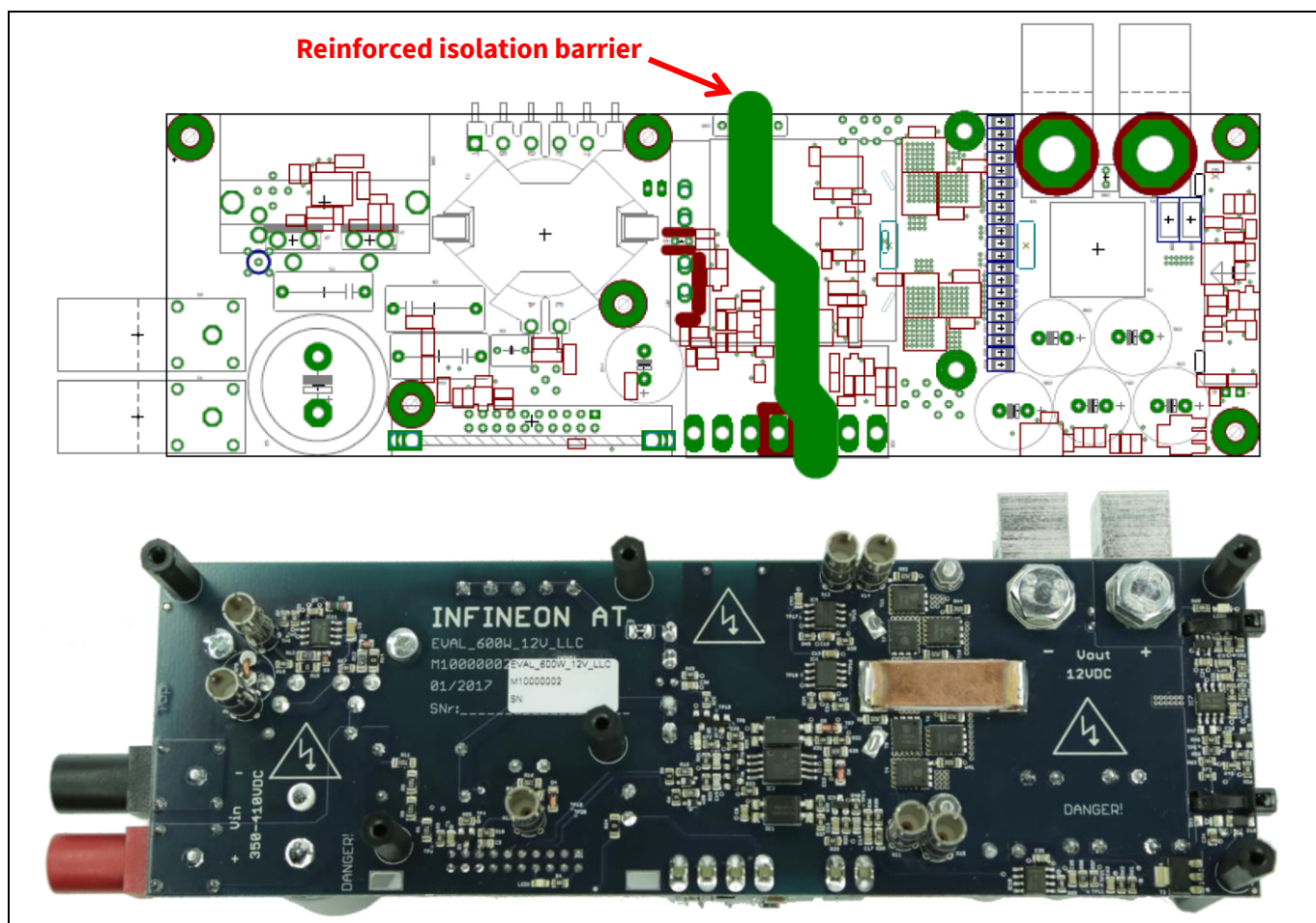


Figure 4 Illustration of the reinforced isolation barrier on a PCB of a resonant LLC converter

Section 2 of this application note presents the most common isolated gate driving solutions and discusses the respective advantages and disadvantages. Section 3 compares the different solutions based on the main parameters and features: isolation level, propagation delay, parasitic leakage inductance, parasitic input-to-output capacitance, CMTI, component size and thickness, PCB layout flexibility and compactness. Finally, the summary and main conclusions are provided in section 4.

2 Isolated gate driving solutions

Several solutions can be used to drive a HB while providing the required galvanic isolation between the controller and the power switches. In this section, the most common approaches are detailed along with the respective advantages and disadvantages. Solution A is based on pulse transformers and is typically used to drive IGBTs and SJ MOSFETs. However, due to its parasitic inductances and capacitances, the pulse transformers are not suitable to drive SiC MOSFETs and GaN HEMTs in applications with high di/dt and dv/dt transients. As an alternative, *Solutions B to F* are based on isolated gate driver ICs and digital isolators, which makes them robust for applications using SJ MOSFETs, SiC MOSFETs and GaN HEMTs. These modern isolated gate driving solutions enable high power density designs with functional, basic or reinforced isolation levels.

2.1 Solution A – pulse transformer

One of the mainstream solutions to drive a HB is based on a pulse transformer. This transformer provides the galvanic isolation between the controller and the power switches in the HB. For basic and reinforced isolation applications, the pulse transformer is mounted on the PCB across the isolation barrier. One of the main advantages of the pulse transformer in this application is no requirement for isolated DC-DC power supplies to drive the MOSFETs. As shown in Figure 5, a dual-channel LS driver IC is used to deliver the high currents needed for charging the gate capacitance of the power switches. The gate-driver IC must have a source/sink output to differentially drive the primary side of the pulse transformer. OUTA is activated during the first half-cycle of the PWM, generating a positive voltage across the primary winding of the pulse transformer. In the other half-cycle of the PWM, OUTB is activated during the same period to provide a negative voltage across the primary winding. Since the magnetizing current of the transformer is added to the gate currents, the output current of the driver can change polarity. Therefore, the output stage of the driver IC must be capable of handling bi-directional current when coupled with a pulse transformer. The EiceDRIVER™ 2EDN [10] has built-in diodes at the output stage to withstand high reverse currents, ensuring high robustness in this application [11]. Furthermore, the source/sink current capability goes up to 5 A/5 A (depending on the package), which fits the needs of the different $R_{DS(on)}$ classes of SJ MOSFETs, SiC MOSFETs and GaN HEMTs.

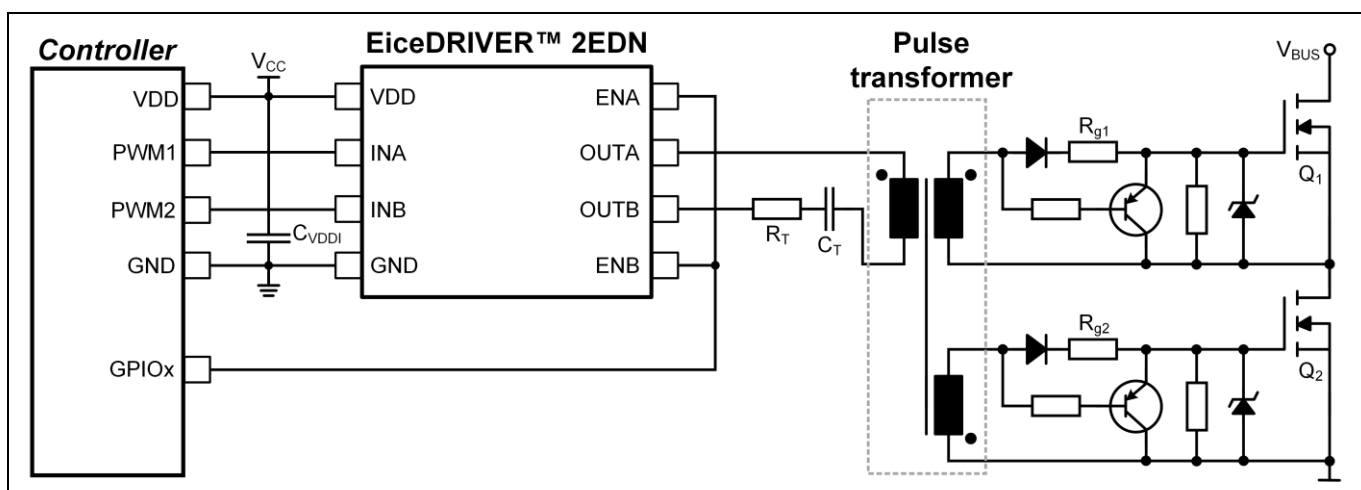


Figure 5 Solution A with a dual-channel LS driver IC and a pulse transformer

The volt-second product applied across the magnetizing inductance must always be symmetrical for any two consecutive half-cycles in order to reset the core flux. This limits the duty cycle to a maximum of 50 percent when using the same driving voltage for turn-on and turn-off. For the LLC topology operating with constant 50 percent duty cycle, this is not a significant drawback. However, for a FB SR on the secondary side, operating with duty cycles in the range of 75 percent to 85 percent, a solution based on pulse transformers cannot be used [12]. Furthermore, and for a specific pulse transformer, the minimum switching frequency is restricted to

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avoid core saturation due to the volt-second limit. For example, the GT06-111-100 [13] has an E-T product of 100 V- μ s, which means that for a 12 V driving voltage the minimum switching frequency is 60 kHz. Therefore, a bulkier pulse transformer with higher E-T product is required, if the switching frequency is lower. In general, the switching frequency for pulse transformers is restricted to a range between 40 kHz and 1 MHz.

The capacitor C_T is typically connected in series with the primary winding of the transformer in order to prevent DC flux “walking” due to small volt-second asymmetries. However, this technique cannot prevent flux saturation due to duty-cycle asymmetry. Moreover, due to the relatively low DC resistance of the primary winding, the voltage drop associated with the DC magnetizing current component is usually not sufficient to cancel the volt-second asymmetry until the core reaches saturation. For that reason, the resistor R_T is also connected in series with the primary winding of the transformer in order to increase the voltage drop associated with the DC magnetizing current component and promote the cancelation of the volt-second asymmetry.

The leakage inductance L_{LK} is another important parameter of the pulse transformer that can significantly affect the performance of this driving solution. It is mainly dependent on the way the windings are arranged inside the available window area of the magnetic core. The L_{LK} of pulse transformers is typically around 0.5 percent of the primary inductance, and can easily reach dozens of μ H. This represents a relatively high impedance for fast-changing signals. Using toroid cores, the leakage inductance can be significantly reduced when compared with other core shapes, but it still typically exceeds 300 nH. Since the input-to-output propagation delay across the transformer is directly related to the leakage inductance, it should be minimized. Let's take one example considering the GT06-111-100 pulse transformer (based on a toroid core) and the 600 V CoolMOS™ CFD7 SJ MOSFET IPB60R105CFD7 [14]:

$$V_{CC} = 12 \text{ V}$$

$$L_{LK} = 470 \text{ nH}$$

$$R_{DS(on)} = 105 \text{ m}\Omega, Q_{gs} = 10 \text{ nC}, Q_{gd} = 14 \text{ nC}$$

Since L_{LK} is in the gate loop, the di/dt is then limited to around 25.5 mA/ns. Assuming the gate resistor is not limiting the current rise, then it takes around 28 ns to charge Q_{gs} and reach the Miller plateau. In a resonant converter such as the LLC, the turn-on occurs under ZVS conditions and the switch is considered on as soon as the Miller plateau is reached. In a hard-switching application, additional charge must be supplied to reach the end of the Miller plateau. In this case, it will take another 15 ns to completely charge Q_{gd} . Therefore, it takes around 43 ns to completely turn on the SJ MOSFET in a hard-switching application. Assuming the EiceDRIVER™ 2EDN with a propagation delay of 19 ns, this solution based on pulse transformers requires around 47 ns and 62 ns respectively in soft- and hard-switching applications to turn on the SJ MOSFET.

In contrast, when using a solution based on an isolated gate-driver IC, the gate loop inductance is mainly dependent on the PCB layout. A typical value for the total gate loop inductance is 10 nH.

Therefore, the significantly higher di/dt transient enables very quick charging of C_{gs} and C_{gd} , which results in almost negligible charging times when compared with the pulse transformer solution.

The leakage inductance should also be minimized in order to avoid problems associated with cross-conduction of the switches, originated by mis-matched propagation delays for the HS and LS windings. The manufacturing tolerances of the pulse transformer should be tight in order to ensure precise timing. Moreover, ringing might occur due to large di/dt of the currents flowing in the leakage inductance. This could lead to spurious turn-on of the gate, which may finally result in shoot-through of the DC-link (V_{BUS}) and eventually even damage of the HB MOSFETs. Therefore the use of pulse transformers is limited to applications with relatively slow current transients.

[illegible]

The magnetic core and the isolated windings of the pulse transformer require a relatively large package which, combined with the gate-driver IC and other discrete components, creates a bulky solution that makes the PCB layout difficult and might be too large for many high-density applications [16]. Furthermore, the height of the transformer is not suitable for the current trend of low-profile SMPS with power modules in parallel using exclusively SMD components. Top-side cooling of SMD power switches is also difficult to implement when a bulky pulse transformer is used for the driving circuit. Finally, the pulse transformers suffer from magnetic property changes and accelerated aging as a function of operating temperature. This could be especially critical in high-density power converters operating at high temperatures, using for example the Infineon CoolSiC™ silicon carbide MOSFET technology [17] capable of operating at a junction temperature up to 175°C.

Galvanic isolation can be integrated in the gate-driver IC using for example Infineon's CT technology. Due to the short distance between the two on-chip transformer coils, a magnetic core is not needed. Functional, basic or reinforced isolation level can be achieved with this technology. For basic and reinforced isolation applications, the package of the gate-driver IC has sufficient creepage and clearance distance to be mounted across the isolation barrier. Figure 7 shows the schematic based on a dual-channel isolated gate-driver IC (e.g. EiceDRIVER™ **2EDS8265H**). The HS channel needs a power supply voltage referenced to the floating ground (phase node of the HB). This power supply can be implemented using a bootstrap circuit (D_B , R_B , C_B) that requires only a few cheap additional passive components when compared with *Solution A*. Alternatively, an isolated DC-DC power supply can be used, which despite being typically more expensive is also a more integrated solution.

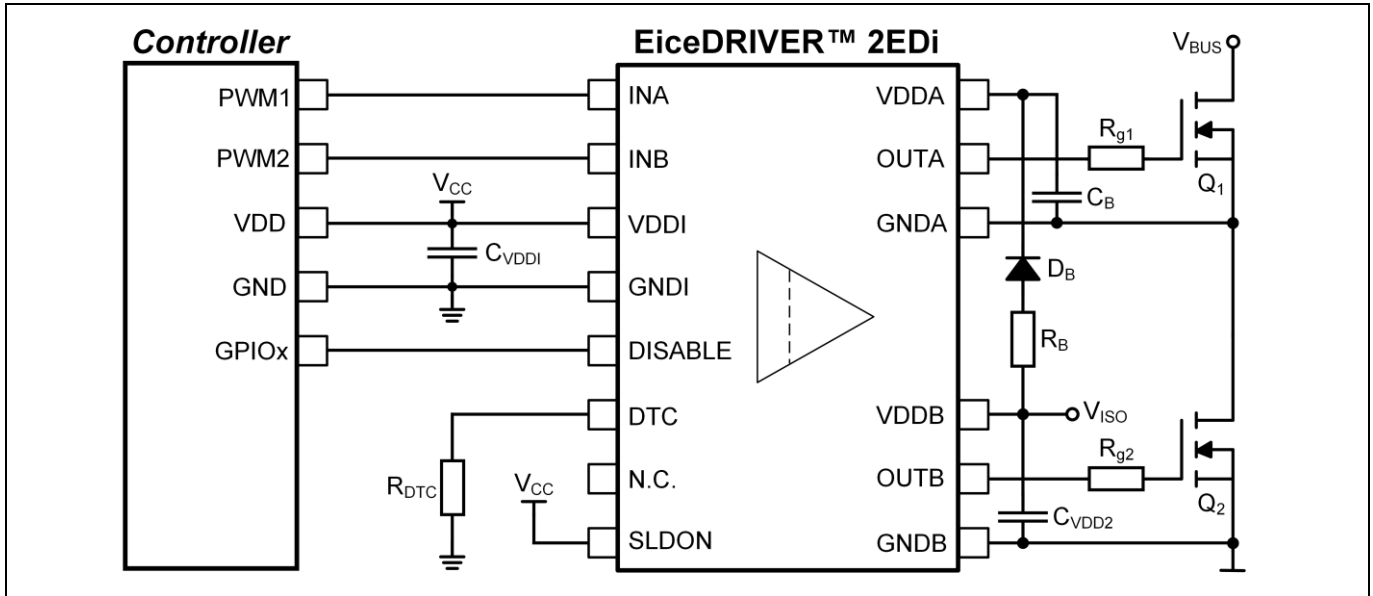


Figure 7 Solution B with a dual-channel isolated gate-driver IC

The EiceDRIVER™ **2EDi** [4] is a family of dual-channel isolated gate-driver ICs providing functional (**2EDFx**) or reinforced (**2EDSx**) input-to-output isolation by means of the CT technology. Due to high driving current capability, excellent CM rejection and fast signal propagation, **2EDi** gate driver ICs are particularly well suited to driving medium- to high-voltage MOSFETs in fast-switching power conversion systems. The propagation delay is similar to or better than that of a pulse transformer (*Solution A*) and the maximum 3 ns channel-to-channel mismatch ensures accurate timing and reliable operation over a wide range of ambient temperatures. The CMTI is a key parameter that determines the robustness of a gate driver. Due to the construction of the CT and the implemented communication protocol, the CMTI capability of the **2EDi** gate driver ICs exceeds 150 V/ns [18], making them able to safely drive SJ MOSFETs, SiC MOSFETs and GaN HEMTs.

Since products based on CT technology do not introduce significant parasitic inductance in the gate loop, the noise induced during a switching event in a HB is almost negligible. This has been evaluated using two versions of the 800 W ZVS PSFB evaluation board [8][19] with the following gate-driving solutions:

- GT05-111-100 pulse transformer and EiceDRIVER™ **2EDN7524F** gate-driver IC (*Solution A*)
- EiceDRIVER™ **2EDS8265H** reinforced isolated gate-driver IC (*Solution B*)

Figure 8 compares the results for the two versions by measuring the gate-to-source voltage of the LS MOSFET during a hard turn-on transition (10 A load) of the HS MOSFET. It is important to stress that, in order to ensure a fair comparison between the two versions of the board, the same transition speed of dV_{DS}/dt of 12.9 V/ns was ensured during the experiment.

The driving circuit based on a pulse transformer (*Solution A*) introduces a significant parasitic inductance in the gate loop that creates ringing due to resonance with the gate-to-source and gate-to-drain capacitances. As can be seen in Figure 8(a), the induced noise on the V_{GS} of the LS MOSFET goes significantly above the threshold voltage of the power switch ($V_{GS(th)} = 4$ V). In order to avoid cross-conduction in the HB due to the significant induced noise, a bipolar voltage driving scheme was implemented in the pulse transformer board. However, higher driving losses result from using a bipolar voltage operation, which affects the overall converter efficiency.

On the contrary, the induced noise during this switching event is almost negligible with the EiceDRIVER™ **2EDS8265H** reinforced isolated gate driver (*Solution B*), as is clearly evident from Figure 8(b). This enables implementation of a driving circuit with a unipolar voltage, since there is no risk of re-turn-on and consequent

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cross-conduction in the HB. Moreover, the lower noise obtained with the **2EDS8265H** driving solution provides some margin to increase dV_{DS}/dt by reducing the gate resistor, thereby speeding up the switching transients and consequently improving the efficiency without compromising robustness and reliability of the converter.

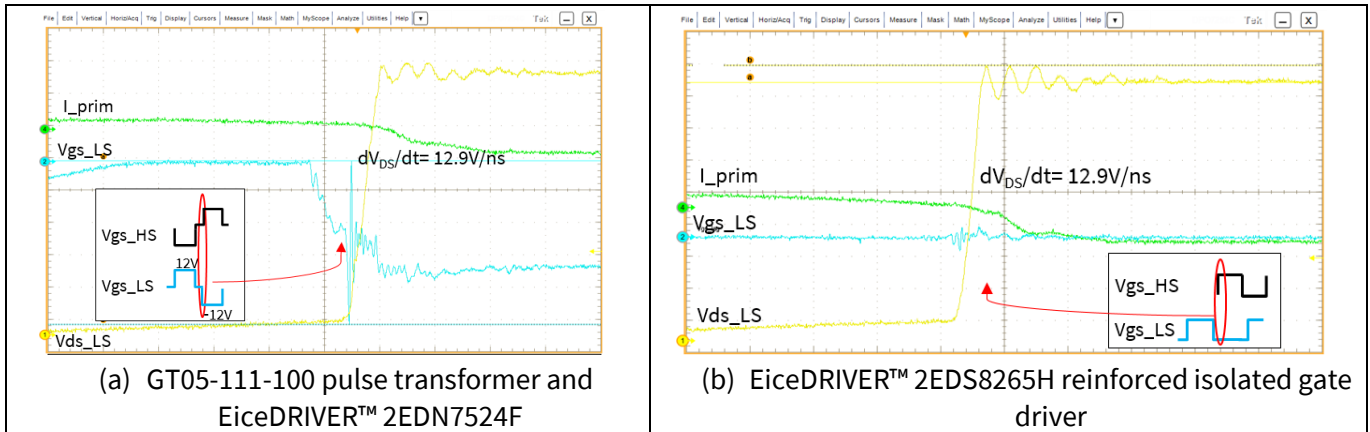


Figure 8 Gate voltage noise during a hard turn-on transition (10 A load) of the HS MOSFET in the 800 W ZVS PSFB evaluation board [8][19]: gate-to-source voltage of the LS MOSFET [cyan], its drain-to-source voltage [yellow] and current in the main transformer [green]. (a) Board with the GT05-111-100 pulse transformer and EiceDRIVER™ 2EDN7524F (*Solution A*). (b) Board with the EiceDRIVER™ 2EDS8265H reinforced isolated gate driver (*Solution B*).

Since the CT is not susceptible to saturation, the duty cycle of the PWM signal can cover the full range from 0 to 100 percent. Furthermore, it is possible to transmit a continuous on or off PWM signal across the gate-driver IC. The maximum switching frequency can typically go up to 10 MHz.

A dual-channel driver also provides additional functionalities, such as Dead-Time Control (DTC) and Shoot-Through Protection (STP) – also known as cross-conduction, overlap or interlocking protection. A fixed dead-time that is added to the PWM signals from the controller can be programmed via an external resistor (R_{DTC}). The STP brings an additional safety layer in case the controller generates wrong PWM signals, increasing the reliability of the conversion system.

As demonstrated in Figure 9, the volume of the main components can be reduced by more than 75 percent by using the EiceDRIVER™ **2EDS8265H** reinforced isolated gate driver when compared with *Solution A*. Obviously the pulse transformer is a bulky component that creates several constraints regarding PCB layout and also mechanical design of the converter. In terms of PCB layout, *Solution B* can ensure the most compact design due to the small size of the driver IC and the need for only a few additional components. Moreover, the small thickness of the driver IC makes it suitable for low-profile SMPS with power modules in parallel using exclusively SMD components. Finally, due to the use of a CT, the EiceDRIVER™ **2EDi** products offer good temperature stability. Therefore, *Solution B* based on a dual-channel isolated gate-driver IC is a highly integrated and reliable solution for high-density power conversion applications using SJ MOSFETs, SiC MOSFETs and GaN HEMTs.

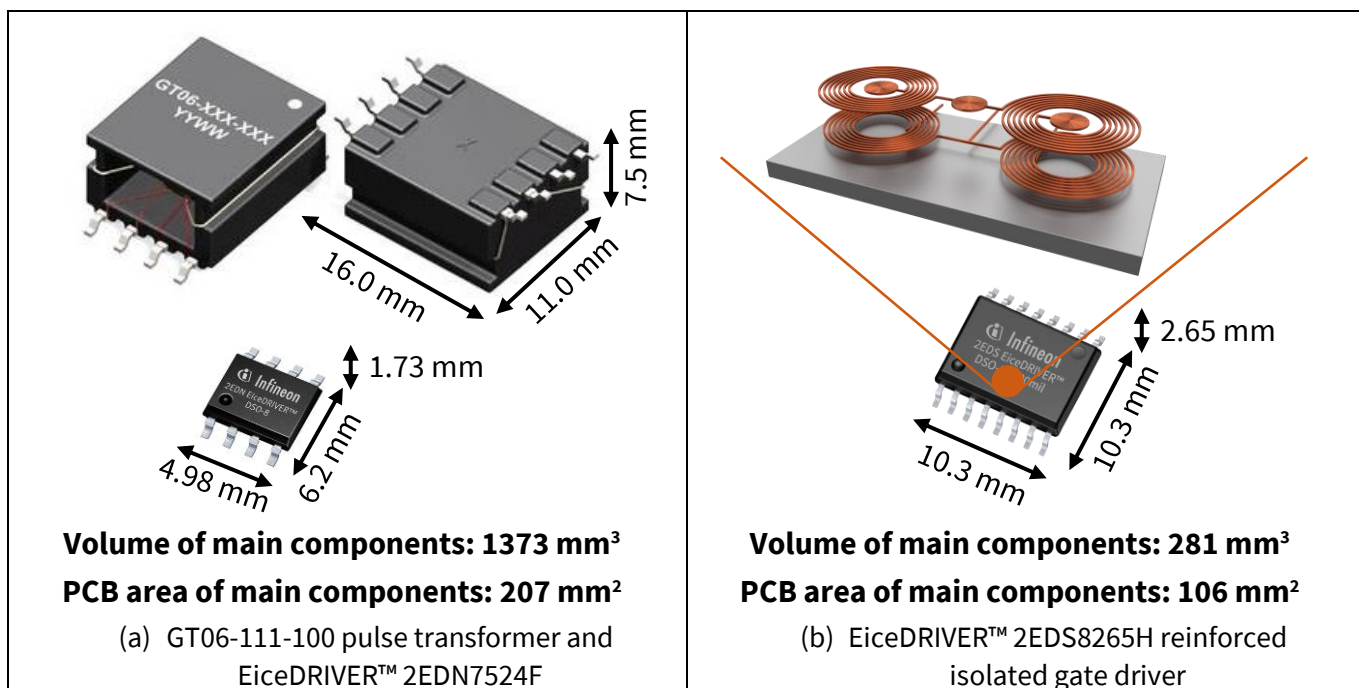


Figure 9 Dimensions, volume and PCB area of the main components of (a) *Solution A* based on GT06-111-100 pulse transformer and (b) *Solution B* based on EiceDRIVER™ 2EDS8265H

2.3 Solution C – digital isolator and a dual-channel isolated gate-driver IC

A different system partitioning can be considered by combining a digital isolator with a dual-channel isolated gate-driver IC. A typical application that uses this driving solution is the isolated DC-DC telecom brick power module. The controller generates the PWM signals that are sent across the isolation barrier by a digital isolator that provides basic or reinforced isolation. This approach enables placement of the driver IC really close to the HB, reducing the parasitic inductances in the gate loop. Figure 10 shows the schematic with the digital isolator as the only additional component when compared with *Solution B*. Since the basic or reinforced isolation is already ensured by the digital isolator, the gate driver IC (e.g. EiceDRIVER™ 2EDF7275F) just needs functional isolation and sufficient channel-to-channel creepage to drive both LS and HS power switches. With this configuration, the designer has a high degree of flexibility in placing the components in the PCB layout.

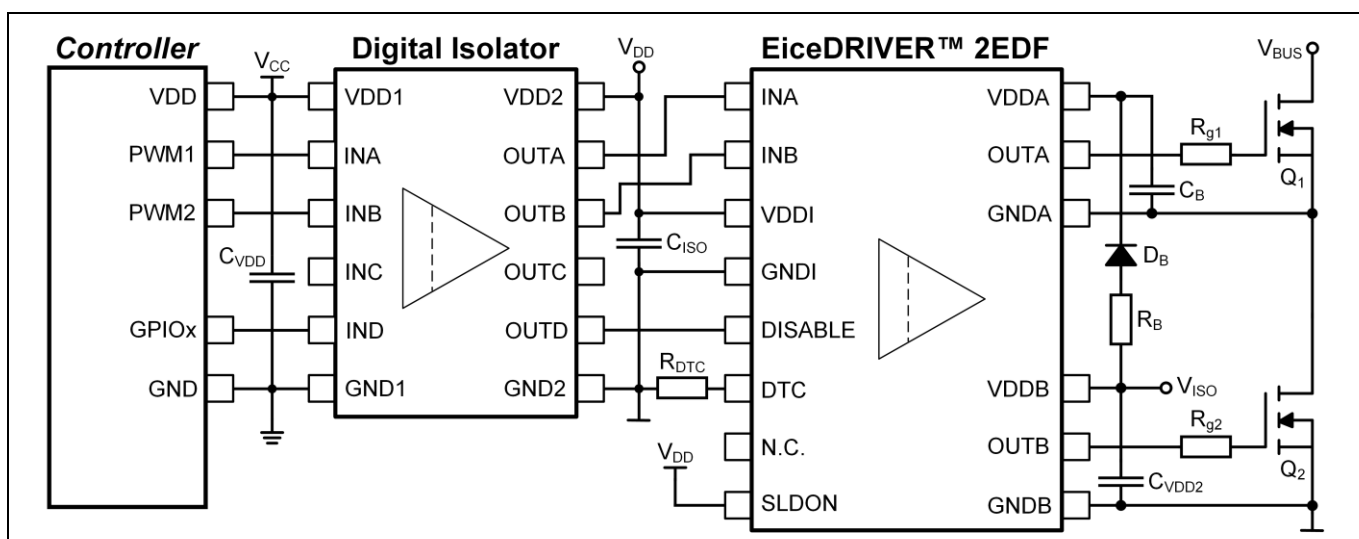


Figure 10 Solution C with a digital isolator and a dual-channel isolated gate driver IC

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The EiceDRIVER™ **2EDFx** is a functional isolated dual-channel gate-driver IC that belongs to the **2EDi** product family [4]. This driver IC is available in an LGA-13 (5x5 mm) and in a DSO/SOIC-16 150 mil (10x6 mm) package. Both versions feature a 1500 V DC functional isolation and support working voltages up to 510 V_{RMS}. Regarding the source/sink current capability, both 4 A/8 A and 1 A/2 A are available to fit the needs of the different R_{DS(on)} classes of SJ MOSFETs, SiC MOSFETs and GaN HEMTs.

2.4 Solution D – two single-channel isolated gate driver ICs

Another solution for the system partitioning could be to use two single-channel isolated gate-driver ICs (e.g. EiceDRIVER™ **1EDB8275F**), as shown in Figure 11. This is an alternative to *Solution B*, with one dedicated gate driver for the HS switch and another driver IC for the LS switch. PCB layout flexibility is increased by making it easier for the designer to place the driver IC closer to the power switch. Additionally, with a dedicated driver for each switch, the trace routing process can also be simplified.

Nowadays, there is a demand for low-profile and high-power-density SMPS for outdoor telecom small cells. The power supply is mounted close to the telecom equipment on a pole or wall. For that reason, the SMPS should be compact in order to cause minimal visual impact, and light to reduce the requirements for the supporting structure and ease the mounting operation. Due to the low maintenance requirement (reduce OPEX) and the necessary IP65 housing, the SMPS should be operated with convection/baseplate cooling (fanless). Therefore, the power stage has to be designed in order to reduce the heat dissipation at full load. There are two possible ways:

- power switches with lower R_{DS(on)} compared to the value used at same P_{out} in case of forced cooling
- interleaving/paralleling of power switches with higher R_{DS(on)} and use of dedicated topologies.

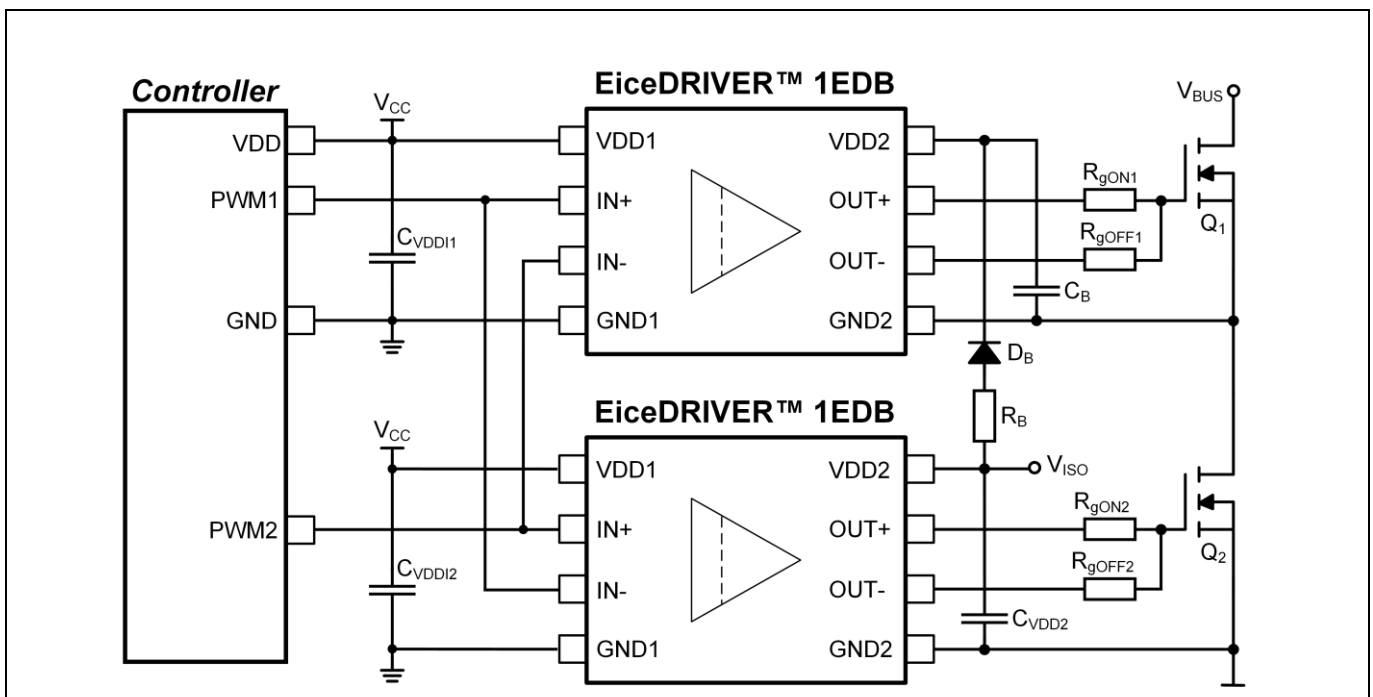


Figure 11 Solution D with two single-channel isolated gate-driver ICs with STP

Having a dedicated gate-driver IC for the HS and another for the LS is preferable when driving an array of paralleled power switches in a fanless SMPS. This approach provides flexibility to arrange the copper areas in order to reduce the parasitic inductance associated with the power loop. Furthermore, routing the traces for all gates of the power switches can also be simplified when compared with a dual-channel gate-driver IC.

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The EiceDRIVER™ **1EDB** [20] is a family of single-channel isolated gate-driver ICs with split outputs and high current driving capability. These features are key to optimize the driving circuit for power switches in parallel. The split outputs (OUT+ and OUT-) enable the customer to use different gate resistors for turn-on and turn-off. This saves one external diode (additional cost and PCB space) that is typically used to provide this flexibility when using gate drivers with a single output. Moreover, the high source/sink current capability (4 A/8 A) enables driving of several medium- to high-voltage SJ MOSFETs, SiC MOSFETs or GaN HEMTs in parallel in fast-switching PCS. As detailed in [21], it is recommended to use individual gate resistors for each power switch in order to provide the necessary damping and gate decoupling to prevent oscillations.

The propagation delay match between the HS and LS gate-driver IC is also important to avoid cross-conduction in the HB. With tight propagation delay variance (+4/-4 ns), EiceDRIVER™ **1EDB** ensures an accurate timing and reliable operation over a wide range of ambient temperatures. Furthermore, this gate-driver IC has non-inverting and inverting inputs (IN+ and IN-) that can be connected as shown in Figure 11 to implement STP. This feature provides an additional safety layer in case the controller generates wrong PWM signals, improving in this way the robustness of the PCS.

2.5 Solution E – single-channel isolated driver IC and the TDI non-isolated gate driver IC

In applications that only require functional isolation, a non-isolated gate-driver IC can be used for driving the LS power switch. This enables the use of a driver IC in a smaller package, which can be beneficial for critically space-constrained applications. For example, an LLC converter commanded by a primary-side PWM controller can use this solution since no basic or reinforced isolation is required. Figure 12 shows the schematic of this solution with a single-channel isolated driver IC (e.g. EiceDRIVER™ **1EDB8275F**) and a non-isolated gate-driver IC with truly differential inputs (e.g. EiceDRIVER™ **1EDN7550B**).

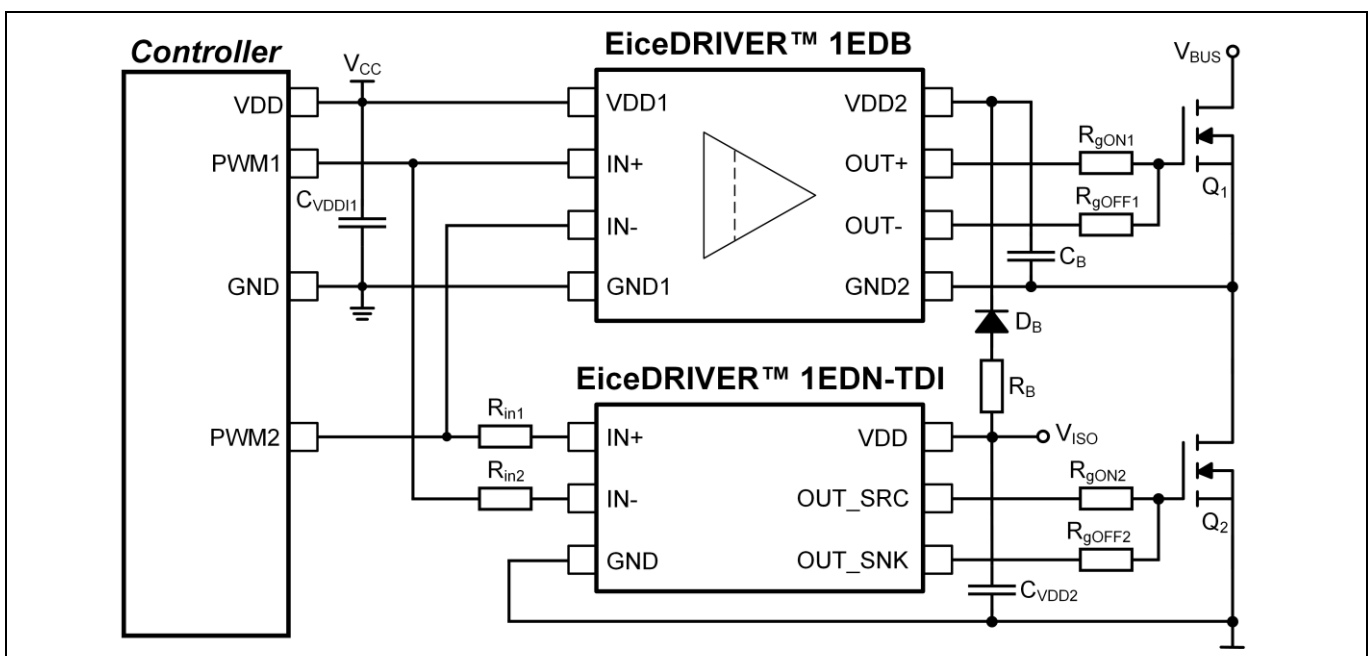


Figure 12 Solution E with a single-channel isolated driver IC and the TDI non-isolated gate-driver IC

The EiceDRIVER™ **1EDN-TDI** [22] is a family of single-channel LS gate drivers with truly differential inputs (TDI) that prevents false triggering of SJ MOSFETs. The control signal inputs are largely independent of the ground potential. Only the voltage difference between its input pins (IN+ and IN-) is relevant. Therefore, this driver IC is a robust solution in applications with AC and DC ground-shift providing the following usable input voltage range:

Isolated gate driving solutions

- dynamic Common-Mode Range (CMR) up to ± 150 V for 3.3 V PWM signals
- static CMR up to -72 V/ $+84$ V for 3.3 V PWM signals

This eliminates the risk for wrong triggering and thus is a significant benefit in all applications exhibiting voltage differences between driver and controller ground, a problem typical for systems with:

- four-pin packages (Kelvin source connection)
- high parasitic PCB inductances (long distances, single-layer PCB)
- bipolar voltage driving schemes.

In the same way as the EiceDRIVER™ **1EDB**, the EiceDRIVER™ **1EDN-TDI** offers split outputs, a high source/sink current capability (4 A/8 A) and the same input-to-output propagation delay (45 ns). For that reason, the combination of both driver ICs is a perfect fit for HB applications requiring just functional isolation. This hybrid configuration is suitable not only for SJ and SiC MOSFETs but also for GaN HEMTs high-voltage half-bridge [23].

2.6 Solution F – dual-channel isolated driver IC and the TDI non-isolated gate-driver IC

A different solution for the system partitioning can be to use a dual-channel isolated and two non-isolated gate-driver ICs. Figure 13 shows the circuit diagram for this solution, where the EiceDRIVER™ **2EDS** [4] is mounted on the PCB across the isolation barrier to provide the required reinforced isolation (e.g. LLC converter controlled from the secondary side). Furthermore, this driver IC also enables the configuration of a DTC feature that is added to the PWM signals from the controller. Additionally, the STP brings an additional safety layer in case the controller generates wrong PWM signals, increasing the reliability of the conversion system.

A dedicated non-isolated gate-driver IC is placed close to each of the power switches in order to reduce the parasitic inductances of the gate loop. The EiceDRIVER™ **1EDN-TDI** [22] is the perfect fit for this purpose, since it comes in small packages (SOT-23-6 and TSNP-6) and with a high dynamic CMR, enabling it to be used even in HS applications. Moreover, the split outputs give flexibility to optimize the turn-on and turn-off performance with different gate resistors. Furthermore, the high source/sink current capability (4 A/8 A) enables driving of several medium- to high-voltage SJ MOSFETs, SiC MOSFETs or GaN HEMTs in fast-switching power conversion systems. Finally, the truly differential inputs prevent false triggering of the power switch, which is especially critical in GaN-based applications with fast transients of the phase node.

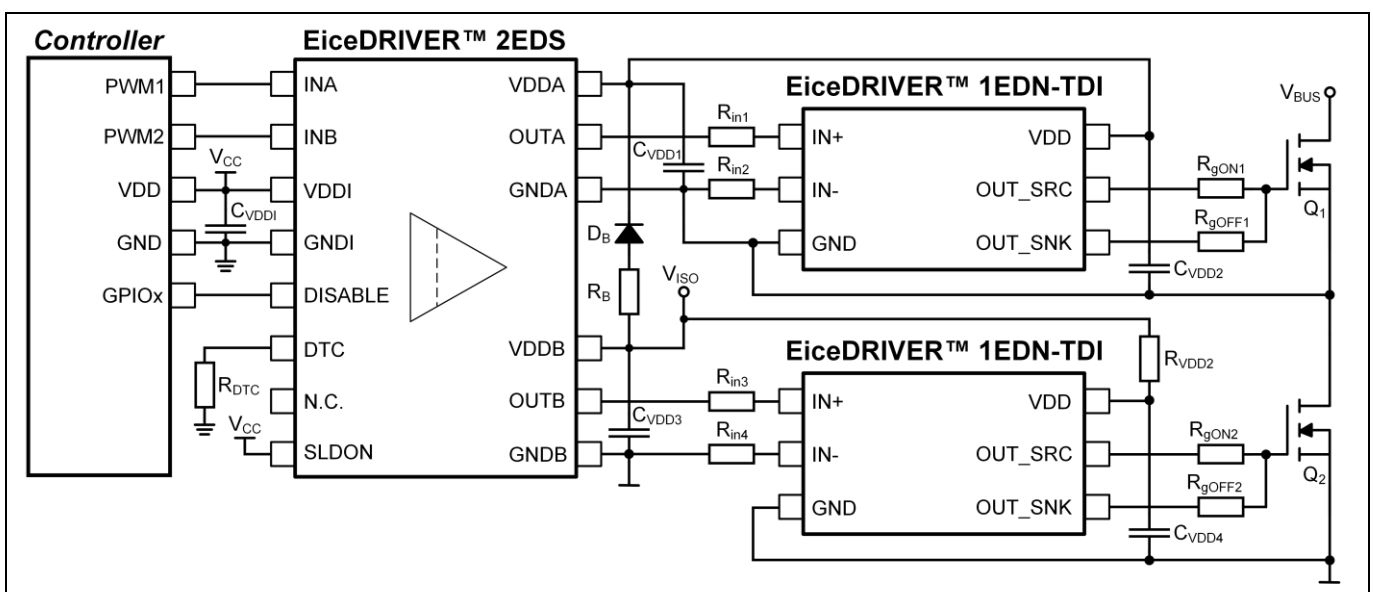


Figure 13 Solution F with a dual-channel isolated driver IC and the TDI non-isolated gate-driver IC

3 Comparison between the isolated gate driving solutions

Having described in the previous section each of the isolated gate driving solutions, it is now important to compare them based on the main parameters and features, as detailed in Table 1. Colors are used to highlight the best (green), average (blue) and worst (red) isolated gate driving solutions for HB configuration.

Table 1 Comparison between the different solutions for isolated gate driving of a HB

Parameter	Solution A	Solution B	Solution C	Solution D	Solution E	Solution F
	Pulse transformer/ "yesterday solution"	Dual-channel isolated gate-driver IC	Digital isolator and a dual-channel isolated gate driver IC	Two single-channel isolated gate driver ICs	Single-channel isolated driver IC and the TDI non-isolated gate driver IC	Dual-channel isolated driver IC and the TDI non-isolated gate driver IC
Isolation level	Reinforced, basic or functional	Reinforced, basic or functional	Reinforced, basic or functional	Reinforced, basic or functional	Functional	Reinforced, basic or functional
Propagation delay	≥ 35 ns	≈ 35 ns	≈ 50 ns	≈ 45 ns	≈ 45 ns	≈ 80 ns
Parasitic leakage inductance (L_{LK})	≥ 300 nH	N/A	N/A	N/A	N/A	N/A
Parasitic in-out capacitance (C_{IO})	≥ 10 pF	≤ 2 pF	≤ 1 pF	≤ 2 pF	≤ 2 pF	≤ 2 pF
CMTI	≥ 50 V/ns	≥ 150 V/ns	≥ 150 V/ns	≥ 150 V/ns	≥ 150 V/ns	≥ 150 V/ns
Duty cycle	≤ 50%	0 to 100%	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Transformer saturation	Yes	No	No	No	No	No
Switching frequency	40 kHz to 1 MHz	0 to 10 MHz	0 to 10 MHz	0 to 10 MHz	0 to 10 MHz	0 to 10 MHz
Component size	Bulky	Small	Small	Small	Small	Small
Component thickness	Large	Small	Small	Small	Small	Small
PCB layout flexibility	Poor	Medium	High	High	High	Best
PCB layout compactness	Poor	High	Medium	High	Best	Medium
Isolated power supply required	No	Yes, or bootstrap	Yes, or bootstrap	Yes, or bootstrap	Yes, or bootstrap	Yes, or bootstrap

Comparison between the isolated gate driving solutions

The achievable isolation level is the first parameter used to compare the different solutions. According to the application requirements, functional, basic or reinforced isolation need to be considered. For example, functional isolation is sufficient for an LLC converter that is commanded from a PWM controller located in the primary side. Therefore, *Solution E* is an option when the HS switch is commanded by a functional isolated gate driver. In case the PWM controller has level-shift capability, the EiceDRIVER™ **1EDN-TDI** can also be used to drive a HS switch [23]. However, the solution with just two EiceDRIVER™ 1EDN-TDIs is not part of the scope of this document. For the LLC converter represented in Figure 3, basic or reinforced isolation are required since the command signals from the PWM controller, located on the secondary side, need to cross the isolation barrier. In this case, *Solution A, B, C, D* or *F* can be used to provide the necessary isolation level.

The propagation delay is a key parameter to compare the different driving solutions. As explained in section 2.1, the leakage inductance of the pulse transformer is in series with the gate loop, and consequently delays the turn-on and turn-off of the switch due to the limiting di/dt. For that reason, the propagation delay of *Solution A* is mainly dependent on the leakage inductance of the power transformer. A minimum value to the propagation delay of *Solution A* is 35 ns, which is equivalent to *Solution B* that is based on a dual-channel isolated gate-driver IC from the EiceDRIVER™ **2EDi** product family. These gate driver ICs have excellent propagation delay accuracy between the two channels which results in improved conversion efficiency [24]. For *Solution C*, another 15 ns need to be considered for the digital isolator in series with the gate-driver IC, resulting in a total propagation delay around 50 ns. *Solution D* and *Solution E* with the EiceDRIVER™ **1EDB** introduce around 45 ns propagation delay. Finally, *Solution F* has one isolated driver IC in series with the EiceDRIVER™ **1EDN-TDI** non-isolated gate driver, which represents around 80 ns of propagation delay.

One of the main advantages of the pulse transformer is not requiring isolated DC-DC power supplies to drive the MOSFETs. On the contrary, *Solutions B to F* need a power supply voltage referenced to the floating ground of the HS switch (phase node of the HB). This power supply can be implemented using a bootstrap circuit that performs the required level shift. An isolated DC-DC power supply is a possible alternative to the bootstrap circuit, but it is typically a more expensive solution.

The high parasitic in-out capacitance (C_{io}) of the pulse transformer is a great disadvantage of *Solution A*, because it reduces significantly the robustness of the converter. It creates a risk of false triggering and shoot-through events, which consequently limits the CMTI capability of this solution to 50 V/ns. *Solutions B to F* have smaller C_{io} values and can easily achieve CMTI capability above 150 V/ns.

The pulse transformer operation can be compromised due to the core saturation as a result of small volt-second asymmetries. This physical limitation of the pulse transformer restricts the maximum duty-cycle to 50 percent, when using the same driving voltage for turn-on and turn-off. It completely prevents the use of pulse transformers in a broad range of applications. Furthermore, the switching frequency is also confined to a range between 40 kHz and 1 MHz. Since the CT is not susceptible to saturation, there is no limit for the minimum switching frequency, which means that a continuous on or off PWM signal can be transmitted across the gate-driver IC. The maximum switching frequency can typically go up to 10 MHz. Moreover, the duty cycle of the PWM signal can cover the full range from 0 to 100 percent. These are clear advantages of using an isolated gate-driver IC that make *Solutions B to F* much better than *Solution A*.

Since the pulse transformer is a bulky component, significant PCB space is required, which consequently reduces the PCB layout compactness. Moreover, the placement of the pulse transformer across the isolation barrier undoubtedly restricts the PCB layout flexibility. The thickness of the pulse transformer also prevents its application in high-power-density designs using several PCBs mounted in parallel using exclusively SMD components.

By contrast, isolated gate-driver ICs can significantly reduce the volume of the driving circuit due to their smaller thickness and footprint size. As a practical example, the EiceDRIVER™ **2EDS8265H** can save up to 75 percent of the volume at the component level when compared with the GT06-111-100 pulse transformer. A gate-driver IC also provides an increased PCB layout flexibility in placing the component across the isolation

Isolated gate driving solutions

Increasing power density and robustness with isolated gate driver ICs

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barrier. In particular, *Solution F* enables the best layout with the minimum parasitic inductances in the gate loop. This is achieved by placing the EiceDRIVER™ **1EDN-TDI** as close as possible to the power switch, while the EiceDRIVER™ **2EDS** is mounted across the barrier to provide the reinforced isolation. In terms of PCB layout compactness, the use of isolated gate driver ICs and digital isolators results in highly integrated and reliable designs that can achieve the best power density.

Summary

4 Summary

There are several isolated gate driving solutions suitable for SJ MOSFETs, SiC MOSFETs and GaN HEMTs. WBG semiconductors bring additional requirements for the driving circuit due to the fast voltage transients and high switching frequencies. Classical isolated gate driving solutions based on pulse transformers can no longer fulfill these requirements. Furthermore, the pulse transformer is a bulky component that creates significant constraints regarding PCB layout flexibility and compactness, compromising its application in high-power-density designs. Modern solutions employing isolated gate driver ICs and digital isolators have a large CMTI capability and are robust against spurious turn-on due to very low parasitic capacitances. Small footprint and low thickness of gate driver ICs and digital isolators enable the best PCB layout in terms of flexibility and compactness. The total system cost can also be reduced due to better Design For Manufacturing (DFM) and Design For Assembly (DFA). Finally, the use of isolated gate-driver ICs and digital isolators results in highly integrated and reliable designs to achieve the best power density for high-performance power conversion applications.

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