Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

RD001 // ELEAZAR FALCO / EMIL NIERGES

1 Overview

This reference design presents an extremely compact auxiliary power supply, providing two isolated output rails of +15 V and -4 V with a combined total output power of 6 W. The design is optimized for driving high-voltage SiC-MOSFET and IGBT discrete devices as well as power modules in high-power converters, and can be easily integrated in the gate driver system. The extremely low interwinding capacitance of the WE-AGDT 750318131 transformer down to 7 pF helps to achieve high CMTI rating (Common-Mode Transient Immunity), enabling with it fast switching speeds, as required by trending applications in areas like e-mobility, renewable energy and industrial automation.

Key Features

- Extremely compact (27 x 14 x 14 mm)
- 4 kV primary-secondary Isolation
- Only 7 pF typ. interwinding capacitance
- PSR Flyback topology with LT8302 (ADI/LT)
- Very tight load/line regulation of 5% typ.
- Up to 86% peak efficiency (83% at 6 W)
- AEC-Q component qualification

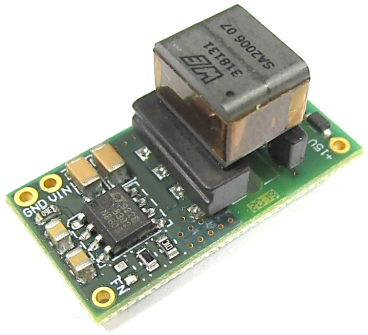


Figure 1: Board Image

Typical Applications

- Automotive powertrain: Traction motor inverter
- On-board and off-board battery chargers
- Industrial drives: AC motor inverter
- Renewable energy: Solar inverters
- Power factor corrector (PFC) stage
- Switch-mode power supplies with SiC MOSFETs

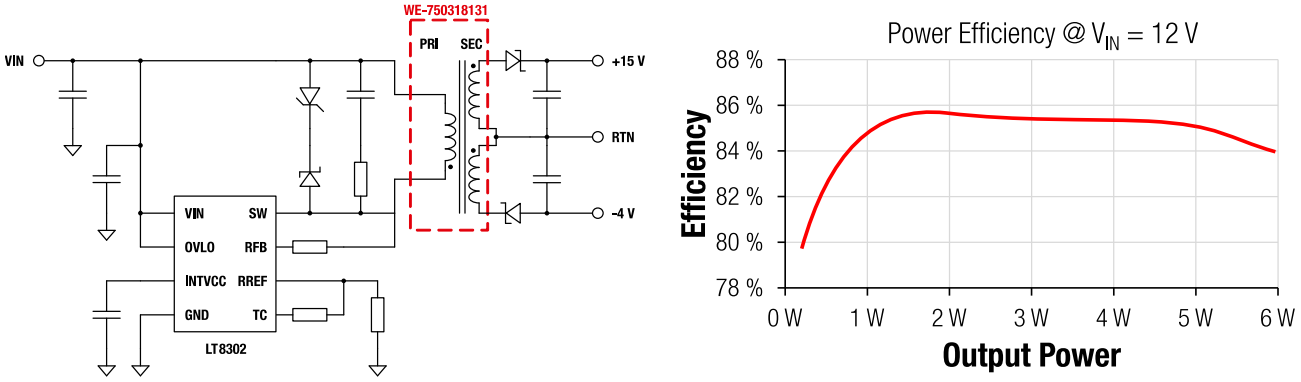


Figure 2: Simplified circuit topology and efficiency at V_{in} (nom) = 12 V

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

2 Technology and System Design Considerations

Silicon Carbide (SiC) technology is enjoying growing popularity in medium and high voltage power switching applications (typically above 300 V). The extremely fast switching speed of SiC-MOSFETs, their low ON-resistance and excellent thermal performance (conductivity and stability) are some of the key advantages against its Silicon-based counterparts. SiC devices are thus starting to replace IGBT (Insulated Gate Bipolar Transistor) and high-voltage Silicon Power-MOSFETs in many applications in industries as diverse as E-mobility, industrial drives and renewable energy.

The voltage required across the gate-source terminals of a SiC-MOSFET are typically found in the range of 14 to 20 V for full turn-on and 0 to -5 V for robust turn-off. Note that a negative voltage is typically used for a faster turn-off transition as well as to keep the device OFF reliably, preventing spurious turn-on caused by parasitic resonant ringing or Miller-effect in hard-switched, half-bridge applications. This is caused by the very high dv/dt generated across the device terminals during fast switching transitions (see section 2.2).

2.1 Gate Driver, SiC-MOSFET and Auxiliary Power Supply System

A low-power isolated auxiliary supply, typically a flyback, push-pull or half-bridge topology, provides the positive and negative output rails, in addition to the required galvanic isolation between the high-voltage and low-voltage sides. This is a requirement not only to meet relevant safety standards, but also to reduce electrical noise as well as to help to improve EMI and gate driver control robustness. The transformer in the auxiliary supply fulfils this primary task. Regarding the gate driver stage, an isolated gate driver IC with an output transistor stage in push-pull/totem-pole configuration is used to drive the gate-source of the SiC device based on a control signal from the controller system. The system connection is shown below:

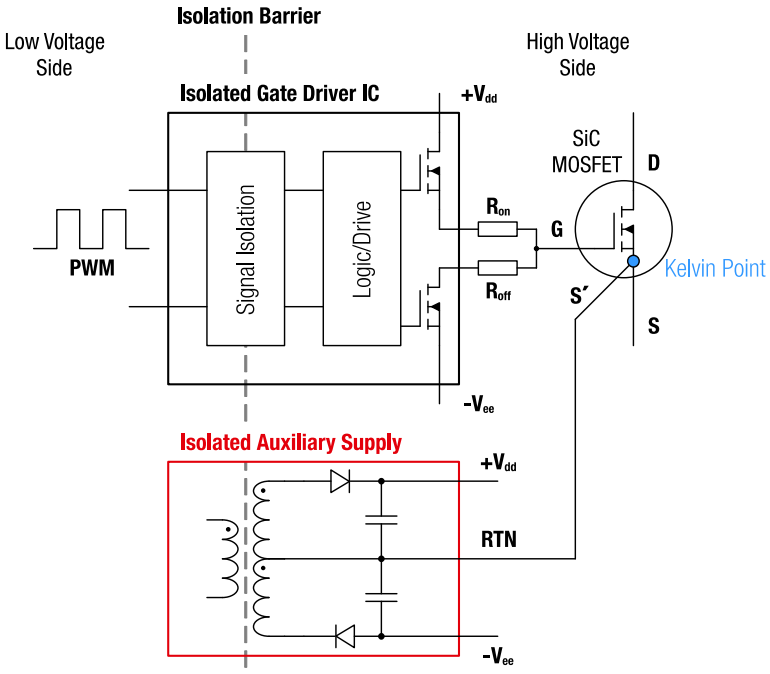


Figure 3: Connection of auxiliary supply with gate driver and SiC-MOSFET

Please note that some SiC devices feature a separate source pin S' (Kelvin connection), which provides a dedicated G-S gate drive current path which is not 'shared' with the current of the power loop (D-S) at the source terminal. This prevents common-source inductance issues during switching transitions, caused by the fast dI/dt of the power loop current causing a voltage drop across the source parasitic inductance which opposes the applied gate drive voltage, slowing down the switching speed. In applications targeting high switching speeds, a '4-pin' SiC device may thus be required.

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

2.2 Why a negative voltage for turn-off of SiC-MOSFETs

A half-bridge SiC-MOSFET configuration is the building block of many switching power converters, with a high-side device and a low-side device switching alternately, and each typically with its own auxiliary power supply and gate driver circuit:

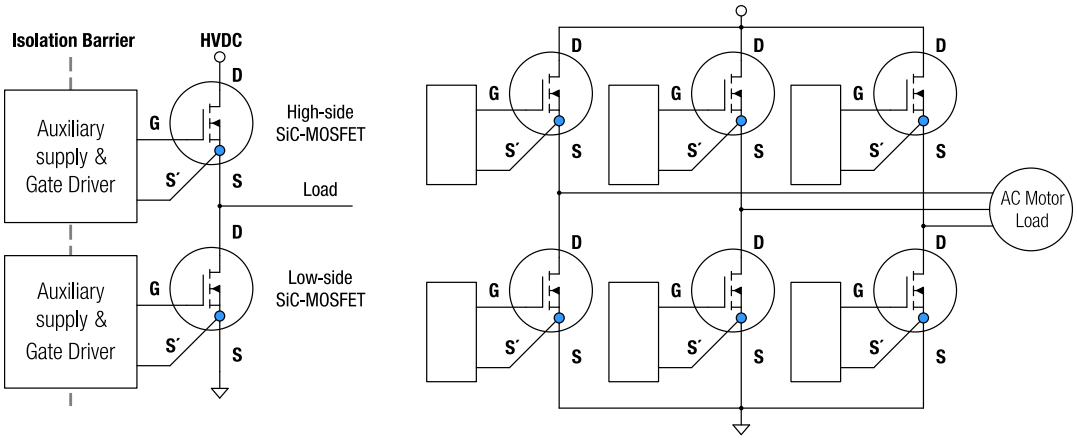


Figure 4: SiC-MOSFET half-bridge configuration (left) and 3-phase inverter application example (right)

When the high-side SiC device is turning ON, the complementary low-side SiC device is already turned OFF as 'deadtime' is used. Deadtime is a short time window during switching transitions where both devices are kept OFF in order to prevent shoot-through or cross-conduction, caused by both devices being turned ON at the same time due to control signal propagation delay mismatch, parasitic ringing, etc. During this 'deadtime', the 'body-diode' of the low-side device keeps current in the loop flowing. On turn ON of the high-side device, the very fast switching speed of SiC-MOSFETs together with the typically high application voltage causes a very high dV/dt to appear across the terminals of the low-side device (Figure 5). This dV/dt in turn causes an instantaneous displacement current to flow through the gate-drain capacitance into the gate of the device. Although the gate-source impedance (Z_{gs}) is a parallel combination of the gate-source capacitance (C_{gs}) with the sum of the total turn-off gate resistance (R_g) and the gate loop inductance (L_p), this approximates for high frequency harmonics the impedance of C_{gs}, and therefore C_{gd} and C_{gs} form an effective capacitive divider. Based on this, C_{gs} should be much higher than C_{gd} in order to prevent the voltage bump generated across gate-source to exceed the threshold voltage of the device, turning it ON as a consequence. This is known as Miller-effect turn-on, causing a shoot-through event with both SiC devices partially ON at the same time, effectively 'shorting' the HVDC supply to GND. This is a very dissipative event with consequences ranging from a drop in efficiency and higher operating temperature up to even catastrophic damage of the devices in severe cases.

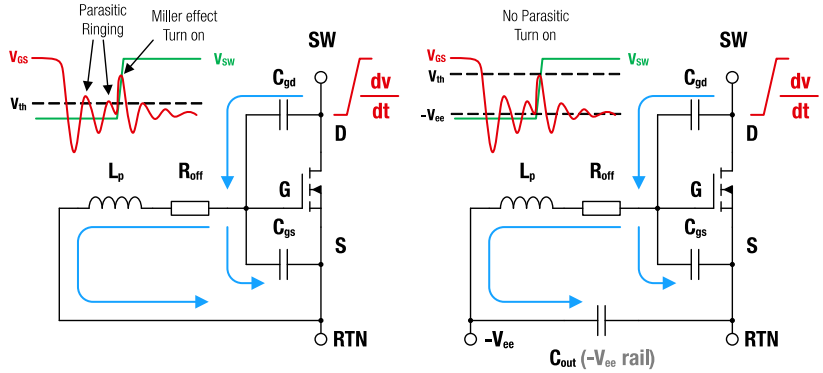


Figure 5: SiC-MOSFET Parasitic turn-on without –V_{ee} rail connection due to Miller effect and gate resonant ringing (left) and with –V_{ee} rail connection (right).

In Figure 5, an example of the Miller effect is shown for the low-side device when the high-side device turns-on. It is observed how a negative gate drive voltage for turn-off provides extended margin to the SiC-MOSFET ON threshold voltage (V_{th}), helping further to prevent spurious turn-on due to Miller-effect and/or parasitic ringing during the very fast switching transitions. A negative gate drive voltage will also help increase the switching speed. There are some particular cases, like in soft-switching applications or when using a gate driver IC with an active Miller clamp, where a negative voltage may not be essential. An isolated auxiliary supply with unipolar voltage can then be used instead.

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

2.3 Auxiliary supply: Output power requirement

During the switching transitions of the SiC-MOSFET device, power is dissipated in the gate current loop resistance as current flows to charge and discharge the gate capacitance of the device to the positive and negative auxiliary supply voltage levels, in order to turn it ON and OFF respectively. The auxiliary power supply of the gate driver system needs to source this power, which depends on the gate voltage, switching frequency and total gate charge of the SiC-MOSFET, as follows:

$$P = Q_g \cdot f_{sw} \cdot \Delta V_{gs}$$

Where:

Q_g: Total gate charge of SiC device for ΔV_{gs} (see Q_g vs V_{gs} curve in SiC device datasheet)

f_{sw}: Switching frequency of SiC device

ΔV_{gs}: Gate-to-source voltage (full-swing) (e.g. for V_{dd} = +15 V and V_{ee} = -4 V, then ΔV_{gs} = 19 V)

The output stage circuitry of some gate driver ICs is powered from the auxiliary power supply rails (i.e. V_{dd}, $-V_{ee}$). This needs to be considered in addition to the previously calculated value and added to the overall power budget of the auxiliary supply.

In Figure 6, it can be observed how during turn-on, the $+V_{dd}$ rail provides the required charge (Q_g) to the gate capacitance (C_g), and during turn-off, C_g discharges via the $-V_{ee}$ rail. Note that there is the same amount of charge flow to and from the gate capacitance (Cg) in a full switching period, leading to the same average current on each rail.

In this reference design, V_{dd} = +15 V and V_{ee} = -4 V and up to 6 W of output power is provided by the auxiliary supply, meaning that each rail sources an average current of around 320 mA. The power contribution of each rail to the total 6 W is different: 4.8 W from the +15 V rail and 1.2 W from the -4 V rail. Each equivalent gate resistance R_{on} and R_{off} dissipate half of the full gate drive power. In this case, for full-load each effective resistance would dissipate 3 W. Please note that the resistance value is not only set by the external resistors added, but also a contribution of parasitic resistances of the internal gate connection of the SiC device as well as ON-resistances of the transistors in the gate driver IC output stage.

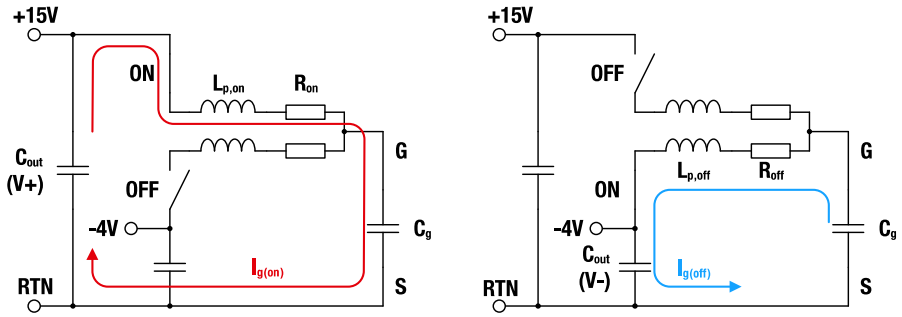


Figure 6: SiC-MOSFET main gate current loops from auxiliary supply output rails for turn-on (left) and turn-off (right)

The turn-on and turn-off resistances (R_{on} and R_{off}) have no effect on the gate drive power requirement. They limit the gate current peak (I_g) during each respective switching transition and in turn, adjust the switching speed of the SiC device. The gate resistances should be minimized together with the respective loop parasitic inductance ($L_{p,on}$ and $L_{p,off}$) in order to achieve high switching speed. This however causes high peak gate currents during the switching transitions and care should be taken to ensure that the gate resistors are sized with adequate pulse power capability in order to dissipate the high instantaneous peak power, as well as the average power as explained above.

Regarding system integration, it is critical to place the auxiliary supply and in particular, the output capacitors, very close to the gate driver and SiC device gate terminal in order to minimize the area of the gate current loop, and with it the parasitic inductance L_p. Multi-layer Ceramic Capacitors (MLCC) like the CSGP series from Wurth Elektronik are also recommended, due to their extremely low package lead inductance L_c and ESR. The paralleling of several capacitors would allow for a higher di/dt of the gate drive current and faster switching speed due to significant reduction of total L_c and ESR. The final value and configuration of the output capacitors should be adjusted by the designer under consideration of switching speed of the SiC device as well as maximum voltage ripple and transient response of the auxiliary supply.

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

2.4 A critical parameter for SiC gate driver systems: Isolation Barrier Parasitic Capacitance

CMTI is the acronym for 'Common-mode Transient Immunity', and it is measured in kV/µs or V/ns. It is an indication of the maximum dv/dt which can be applied across the isolation barrier of the gate driver system before malfunction occurs, causing loss of control of the SiC device and erratic behavior of the system. The CMTI rating directly depends on the parasitic capacitance across the isolation barrier.

The different isolated gate driver ICs in the market use different techniques to transfer the control signal information across the isolation barrier (i.e. capacitive coupling, magnetic coupling, optocoupler, etc). In the auxiliary power supply, the supply energy is transferred via the magnetic field using a transformer. In both cases, a parasitic capacitance exists across the isolation barrier. The high dv/dt appearing across this capacitance (C_{pt}) will generate a displacement current ($i_d(t)$) between the high-voltage power converter side and the low-voltage controller side, as follows.

$$i_d(t) = C_{pt} \frac{dv_{ps}}{dt}$$

A too high displacement current may cause several issues in the system. In addition to distortion of control signals, loss of control of the SiC device due to unpredictable behavior caused by high common-mode signals stressing the controller is also a possibility, in all cases severely compromising basic functionality of the application. The lower the parasitic capacitance, the lower the generated displacement current for a set dV/dt, helping the system to overcome these issues. This in turn also enables higher switching speeds, which are one of the main advantages of SiC devices, since by switching faster, higher efficiency, a smaller overall solution size and a lower system cost of the power converter can be realized. Therefore, the parasitic capacitance across the isolation barrier, which is a contribution of both the auxiliary supply transformer interwinding capacitance and isolated gate driver IC, should be minimized in order to profit from the advantages that the very fast switching speed of SiC devices can offer.

The extremely low interwinding capacitance of the WE-AGDT Transformer series from Würth Elektronik down to 6.8 pF helps the full gate driver system to achieve CMTI ratings above 100 kV/µs as required by many state-of-the-art SiC applications.

In addition to the functional aspects, it is also important to note that the high dv/dt is not only applied between the SW node and DC nodes like DC-Power and system ground (GND) on PCB, but also between the high dv/dt metallic nodes in the circuit board and Earth potential (to which the product chassis might be connected). This generates common-mode displacement currents across the isolation barrier parasitic capacitance, adversely affecting EMI performance. The lower the parasitic capacitance C_{pt} across the isolation barrier, the higher the impedance presented to any common-mode noise currents coupling between the HV and LV sides (see Figure 7).

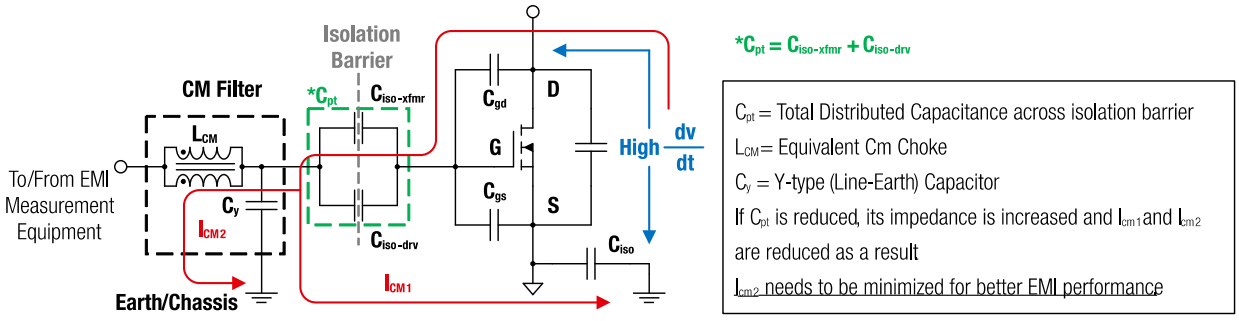


Figure 7: Simplified example of common-mode noise current coupling path for EMI considerations

As a result, improved EMI performance, especially in radiated emissions frequency spectrum, as well as a lower attenuation requirement for the common mode input EMI filter can be expected.

For further information on SiC gate driver system considerations, please also refer to the Application note ANP082 on we-online.com/ANP082

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

3 Electrical Specification

	Minimum	Nominal	Maximum	Units
Input Voltage	9	12	18	(V)
Output Voltage (+)	14.8	14.9	15.6 (*)	(V)
Output Voltage (-)	-4.1	-3.85	-3.75 (*)	(V)
Output Current (per rail)	3		320	(mA)
Output Power			6	(W)
Switching Frequency (**)	80		360	(kHz)

Table 1. Electrical specification table

NOTE: Specification at 25 °C ambient temperature

(*) When using clamping zeners for minimum load as per section 11 (BoM). Note that minimum load resistors can also be used to set output voltage levels under 'no-load' condition.

(**) Switching frequency varies with load current and input voltage.

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

4 Schematic

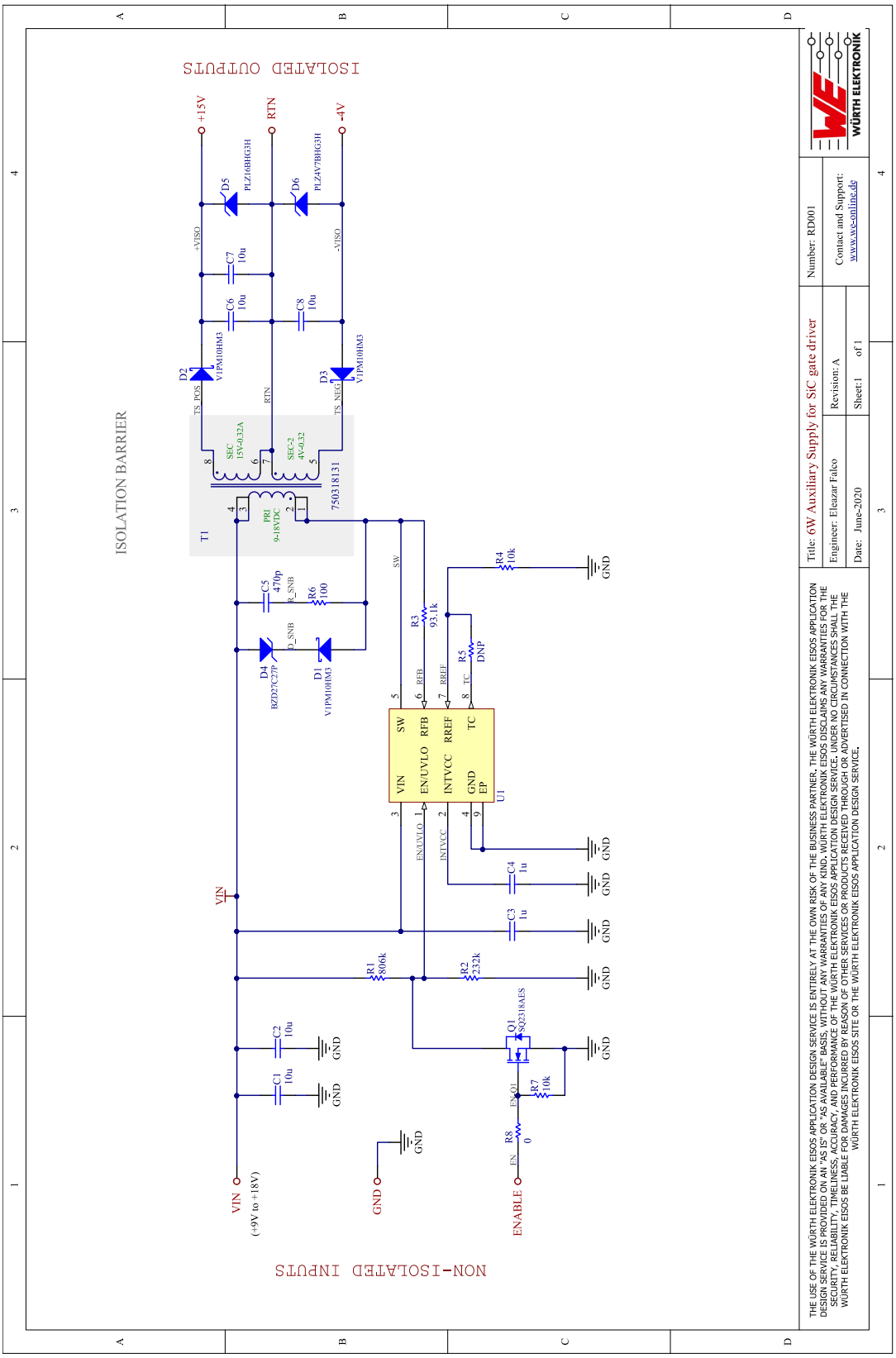


Figure 8: Schematic

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

5 WE-750318131 transformer characteristics

Würth Elektronik has designed a new transformer with optimal characteristics to be used in this PSR Flyback converter reference design to drive high-performance SiC-MOSFET devices.

Finding an optimal converter operating condition to achieve the smallest transformer size and at the same time high efficiency, good thermal performance and compliance with relevant safety standards were the key design objectives. The WE-AGDT 750318131 transformer uses a very compact EP7 assembly, 4 kV isolation voltage, overvoltage category II, pollution degree 2, fully insulated wire (FIW) and creepage/clearance distances according to standards IEC62368-1 and IEC61558-2-16. Additionally, it counts with AEC-Q200 qualification.

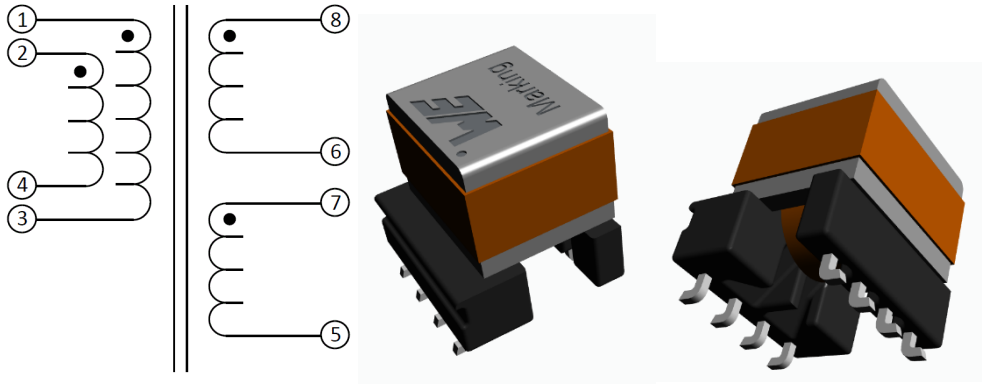


Figure 10: WE-750318131 Transformer details

Parameter	Test conditions	Value
DC resistance – primary	tie(1+2, 3+4), +20 °C	0.047 Ω ± 15%
DC resistance – Sec.1	8-6, +20 °C	0.205 Ω ± 15%
DC resistance – Sec.2	7-5, +20 °C	0.071 Ω ± 15%
Magnetizing inductance	10 kHz, 100 mV	7.00 µH ± 10%
Saturation current	20% roll-off of L_{mag}	4.5 A (min.)
Leakage inductance	100 kHz, 100 mV	270 nH (typ.)
Interwinding capacitance	100 kHz, 10mVAC	7.5 pF (typ.)
Dielectric	4000 VAC, 1 second	4000 VAC, 1 minute
Partial discharge	1000 V_{pk}, 5 sec. 800 V_{pk} 15sec.	10 pC
Turns ratio	(1-3):(2:4)	1:1 (±1%)
Turns ratio	(8-6):(1:3)	1.55:1 (±1%)
Turns ratio	(1-3):(7:5)	2.2:1 (±1%)
Temperature range		-40 °C / +130 °C

Table 2: WE-750318131 transformer characteristics

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

6 Board layout variants

This reference design is provided in two layout variants: a two-layer single-sided and a four-layer double-sided solution, as well as with two component assembly options: Standard and with AEC-Q qualified components.

6.1 Board layout variant A: Double-sided design

This variant is a four-layer design with all-SMD (surface mount) component assembly on top and bottom sides.

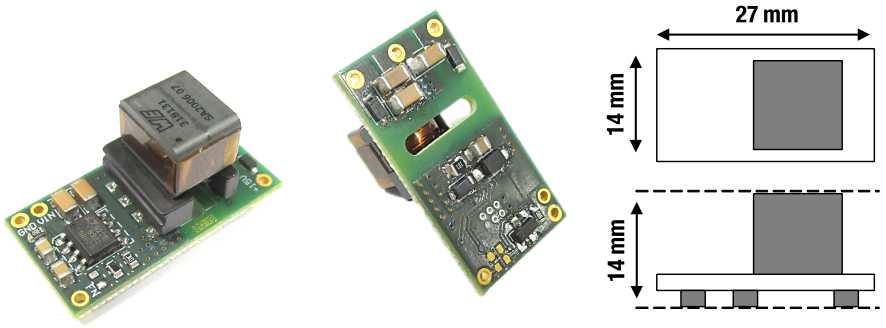


Figure 11: Board variant-A (a) top view (b) bottom view (c) dimensions

6.2 Board layout variant B: Single-sided design

This variant is a two-layer design with all-SMD (surface mount) component assembly only on top side.

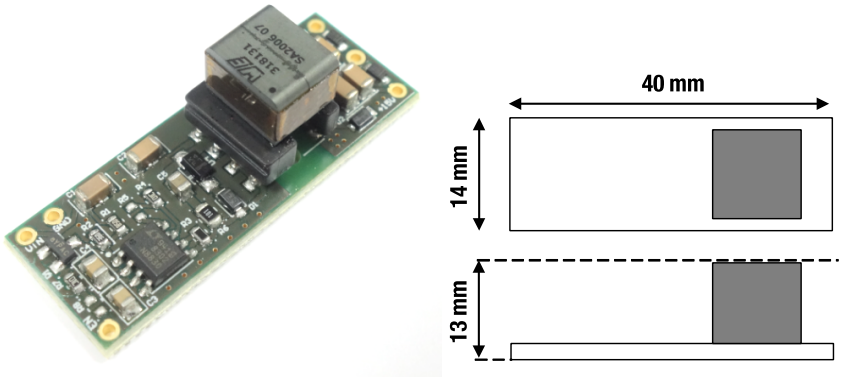


Figure 12: Board variant-B detail and dimensions overview

NOTE: No significant performance difference has been observed or can be expected between the two board layout variants, be this functional, thermal or regarding EMC behaviour. The selection of the variant to use can therefore be made based only on the particular constraints of the application. The compact layout lends itself optimally to integration onto a larger board together with the full gate driver system.

The PCB Layout design files are available (Altium Designer) on we-online.com/RD001.

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

7 Experimental results

7.1 Experimental test setup

The power supply has been tested for functional performance using two electronic loads configured in constant-current (CC) mode. Alternatively, resistive-mode of electronic load or discrete power resistors drawing balanced current on both rails can also be used. Tests are carried out at 25 °C ambient temperature.

7.1.1 List of equipment required (and used in this case)

- 1 x Laboratory power supply (min. 25 V/1.5 A) (used EA-PSI 9040-40 T)
- 4 x 4-digit precision multimeter (it was used instead a Yokogawa WT3000E precision power analyzer)
- 2 x electronic loads (25 V/1 A min.) (used EA-EL 9080-45 T)
- 1 x oscilloscope (4 channel, 350 MHz or higher) (used Keysight InfiniiVision DSO-X-3034T)

NOTE: A precision power analyzer (min. 3-channel) can be used as an alternative to the four multimeters for highly-accurate voltage and current measurements.

7.1.2 System setup

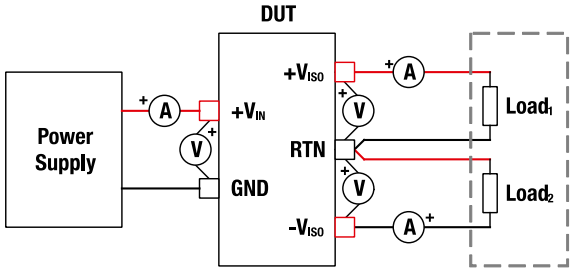


Figure 13: Example of test setup configuration

NOTE: When testing the power supply as described here, both channels must be loaded with the same average current (balanced load). This current emulates the charge flow per second between the gate capacitance of the SiC-MOSFET and the respective output rail when switching (+15 V rail for charging and -4 V for discharging). The average current will increase with switching frequency and SiC-MOSFET total gate charge (i.e. capacitance), with a maximum considered in this design of up to 320 mA per rail.

7.2 Load and line regulation

The output power can reach up to 6 W for this reference design. In addition, the input voltage range is 9 V to 18 V. The line and load regulation results show how each output voltage rail varies with variations in the input voltage and output power, respectively.

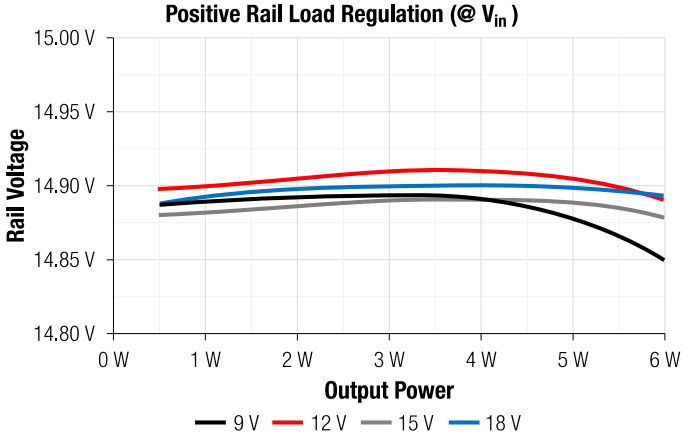


Figure 14: Load and line regulation of output positive rail

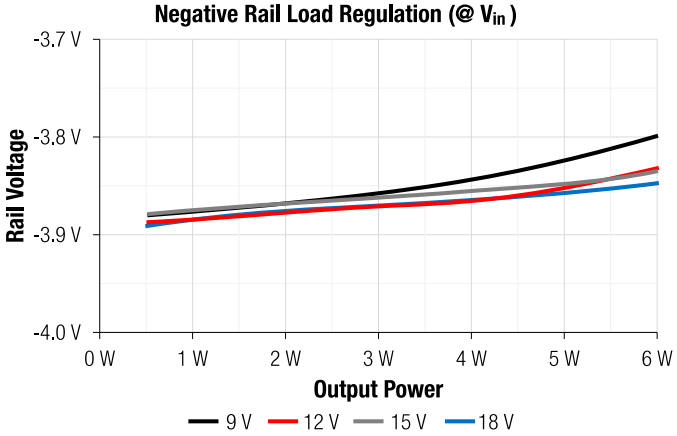


Figure 15: Load and line regulation of output negative rail

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

7.3 Minimum-load line regulation

The LT8302 IC controller requires a minimum load current in order to keep the output voltage regulated, preventing it from steadily increasing at no-load condition. This requirement can be met by using minimum-load resistors or alternatively clamping Zener diodes. The value of minimum load resistors can be adjusted to provide more accurate voltage level at no-load. Clamping Zener diodes are already used at the output for overvoltage protection and they can fulfil the additional role of minimum load current sinking as well.

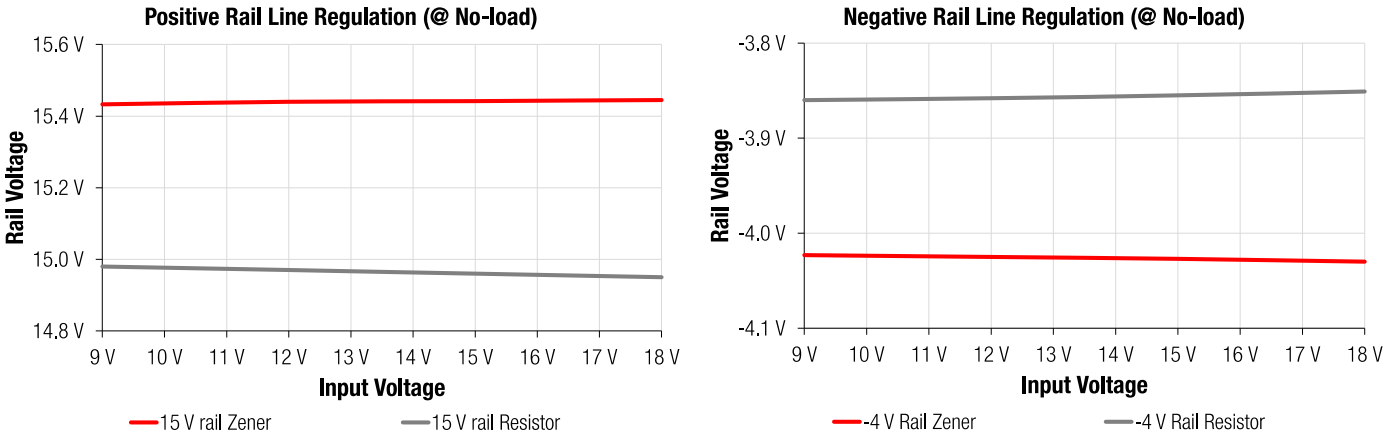


Figure 16: Minimum load line regulation on positive rail (left) and on negative rail (right)

7.4 Power efficiency vs input voltage

Nearly 86% peak efficiency and 84% efficiency at 6 W (full-load) at nominal input voltage is observed.

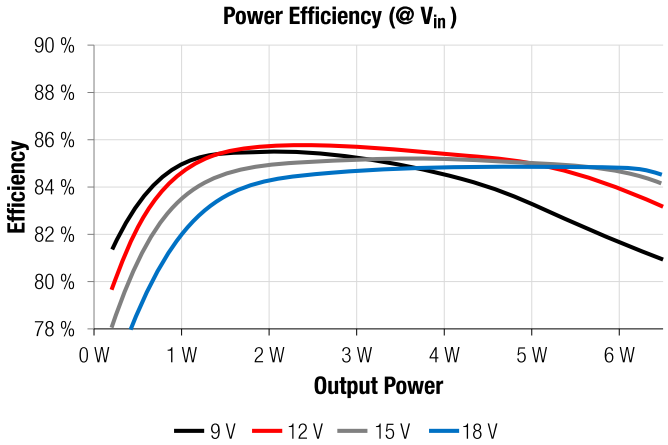


Figure 17: Power efficiency curves

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

8 Main waveforms, oscilloscope captures

8.1 Start-up and shut-down (@ full-load)

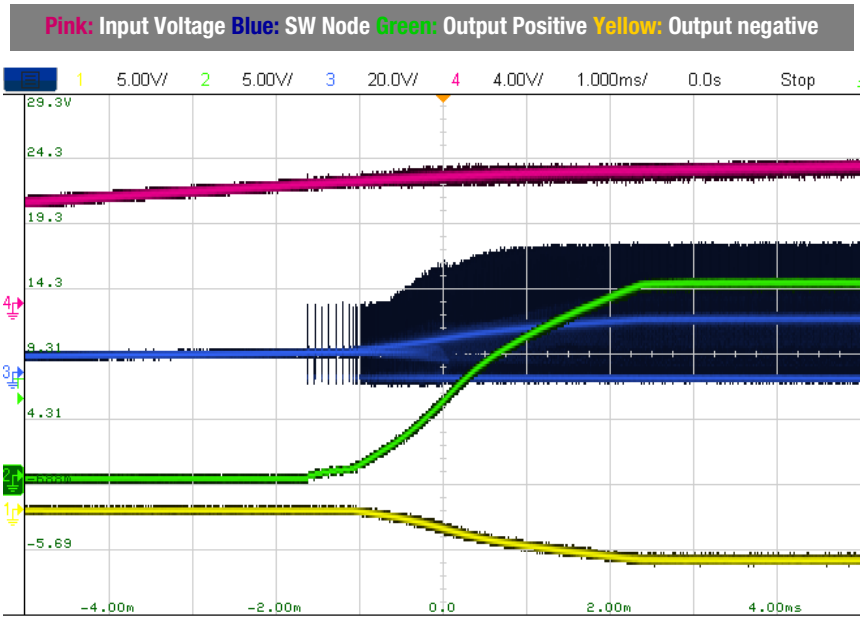


Figure 18: Start-up at full-load

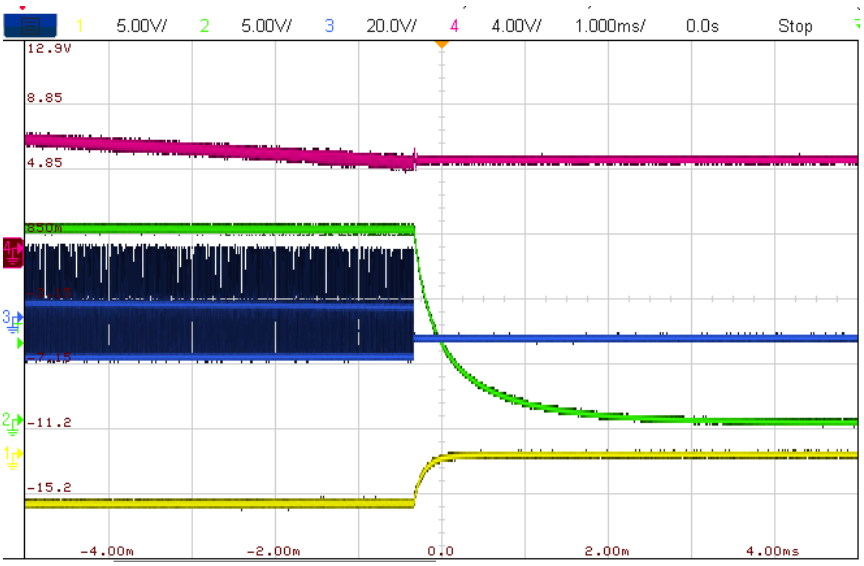


Figure 19: Shut-down at full-load

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

8.2 Steady-state operation

8.2.1 Operation mode with load power

Below transformer primary current and SW node characteristic for 1 W and 6 W loads. At lower loads the Flyback auxiliary supply will operate in discontinuous conduction mode (DCM) (Figure 20), whereas as the output power increases, it will eventually enter boundary conduction mode (BCM) operation (Figure 21).

Figure 20: 1 W load (DCM operation)

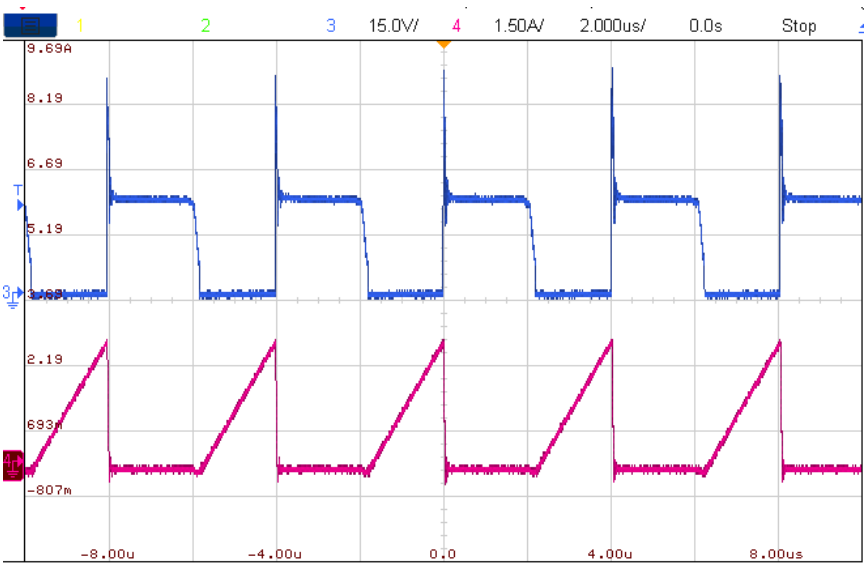


Figure 21: Full load (6 W) (BCM operation)

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

8.2.2 SW node clamping and damping snubbers

The SW node voltage must be kept under 65 V (IC integrated MOSFET rating) and any ringing appearing after the MOSFET turns OFF must be fully damped before 250 ns in order for the LT8302 to correctly sample and regulate the output voltage. The worst-case condition for maximum peak voltage clamping is at the maximum input voltage (18 V) and full-load (6 W). Regarding ringing damping, the worst-case corresponds to the minimum input voltage (9 V) and also full-load (6 W). Oscilloscope captures below under an overload of 6.5 W show maximum SW node voltage of 57.7 V and ringing fully damped before 200 ns, which meets the requirements providing additional margin for variations caused by part-to-part tolerances and operating temperature deviations.

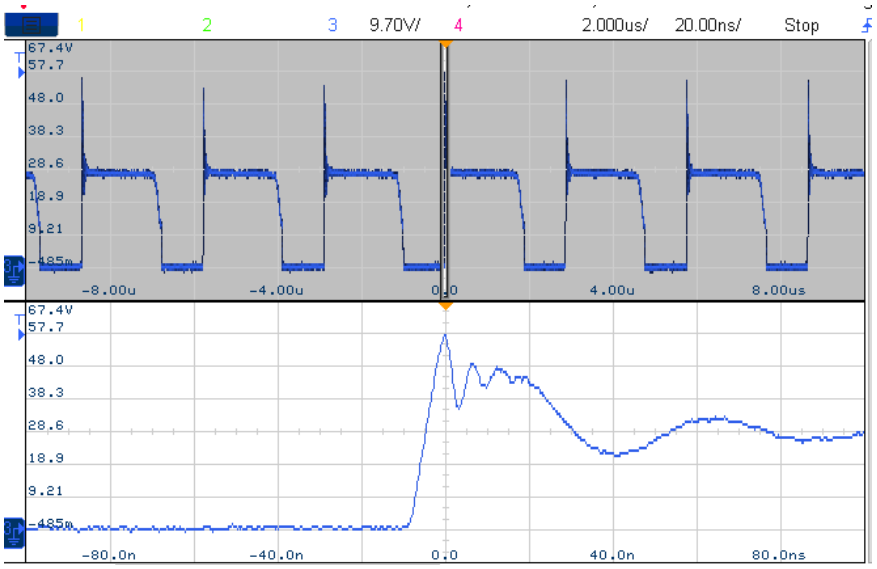


Figure 22: SW Node voltage clamping (Vin = 18 V, P = 6 W)

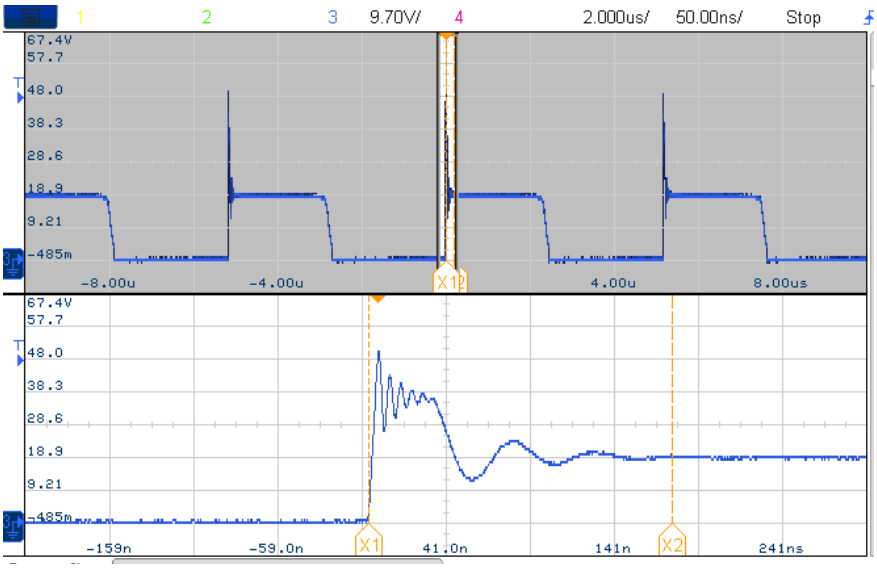


Figure 23: SW Node ringing damping (Vin = 9 V, P = 6 W)

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

8.2.3 Output voltage ripple (at full load)

The output voltage ripple amplitude at nominal V_{in} = 12 V and full load condition is 250 mVpp for the positive rail (under 2%) and 180 mVpp for the negative rail (under 5%). A very cost-effective solution using the same input and output capacitors has been implemented in this reference design. As mentioned in 2.3, this can be modified by the designer as desired, adding more capacitance to further reduce the voltage ripple or increase dI/dt.

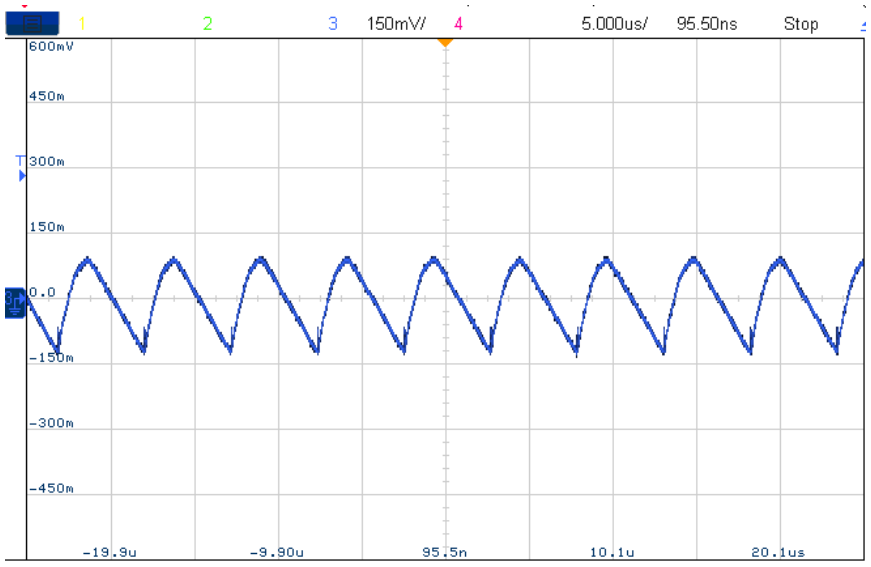


Figure 24: ΔVout. Positive rail (12 V_{in}, 6 W)

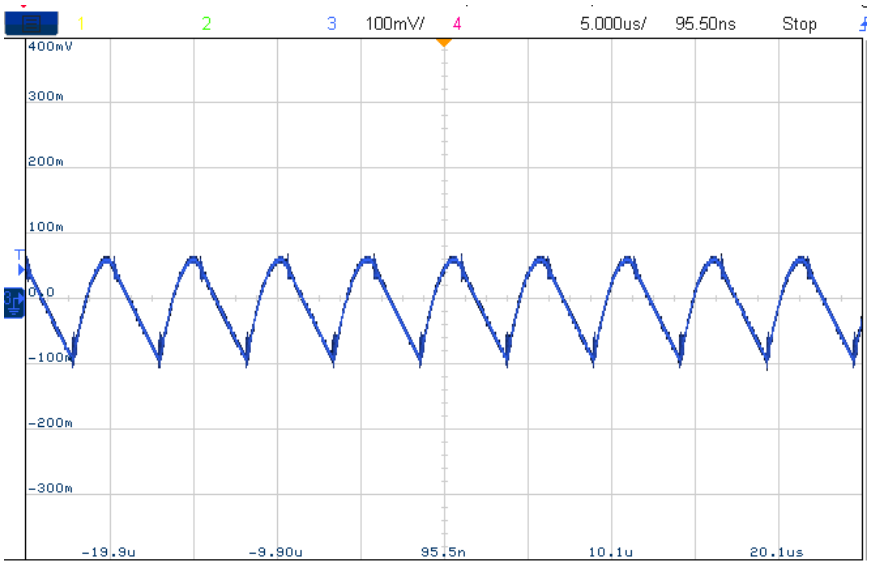


Figure 25: ΔVout. Negative rail (12 V_{in}, 6 W)

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

8.2.4 Load short-circuit and Over-current protection

An overload condition would represent a scenario of a fault in the system, which can be caused, for instance, by the SiC-MOSFET device failing short-circuit across gate and source. This would present a continuous resistive load to the auxiliary supply (instead of mostly capacitive as in normal operation) corresponding to the equivalent gate loop resistance. But since this resistance is typically of very low value, it will draw high current from the auxiliary supply. In this situation, the LT8302 controller will enter hiccup short-circuit protection mode, limiting maximum peak currents. Experimental results under this fault condition show maximum peak current limited to 4.65 A (LT8302 limit), and maximum switch voltage peaking at 62 V, both within ratings of WE-AGDT transformer and LT8302 integrated MOSFET. This improves reliability and robustness of the application as additional upstream damage to the gate driver auxiliary supply can be prevented even under a fault in the main power converter.

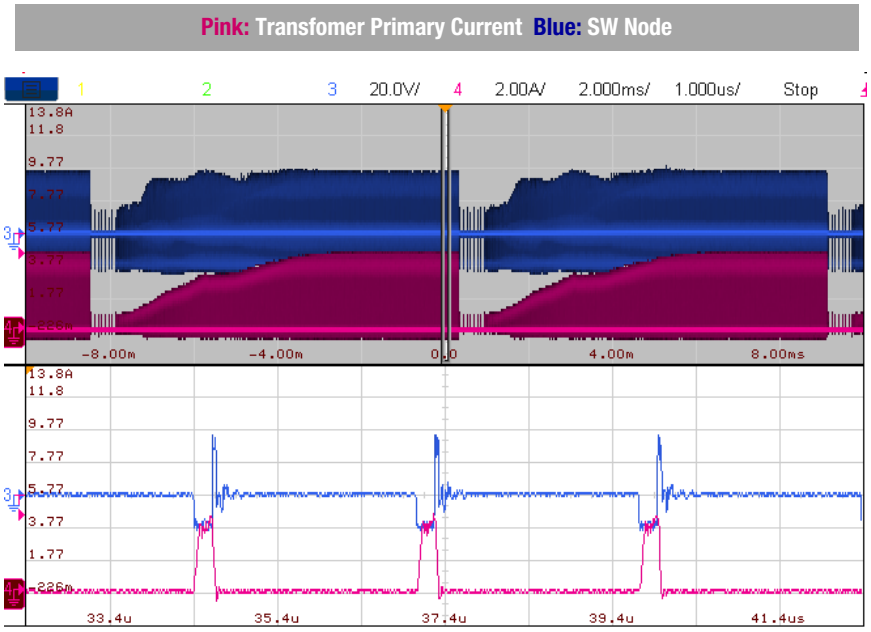


Figure 26: Short-circuit protection at V_{in} = 9 V

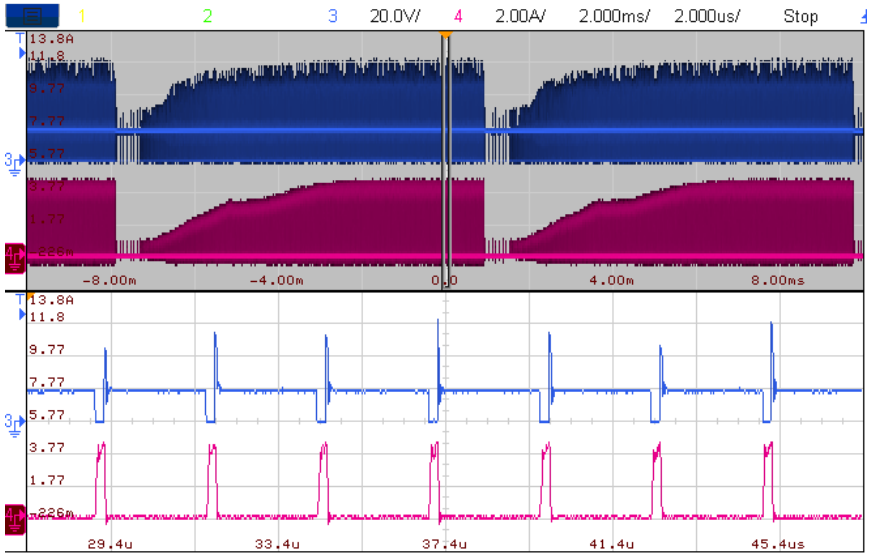


Figure 27: Short-circuit protection at V_{in} = 18 V

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

9 Thermal performance

Thermal performance results over the full-load range (0.1 to 6 W) at minimum input voltage (V_{in} = 9 V) are shown in this section. The results correspond to layout Variant-B board, but the thermal performance of Variant-A shows no appreciable difference.

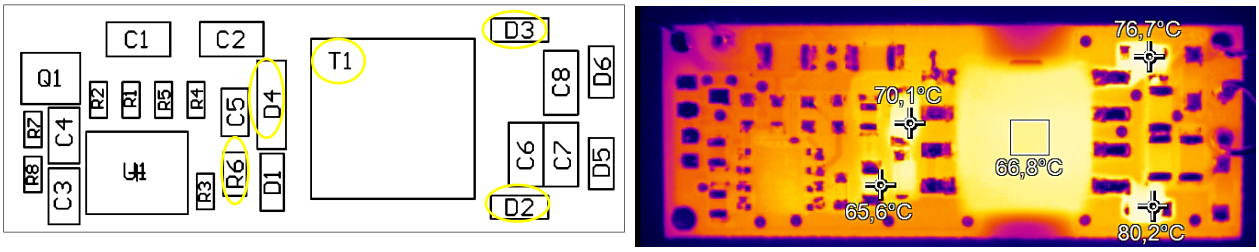


Figure 28: Board components temperature at V_{in} (min) = 9 V (worst-case) and 25 °C ambient

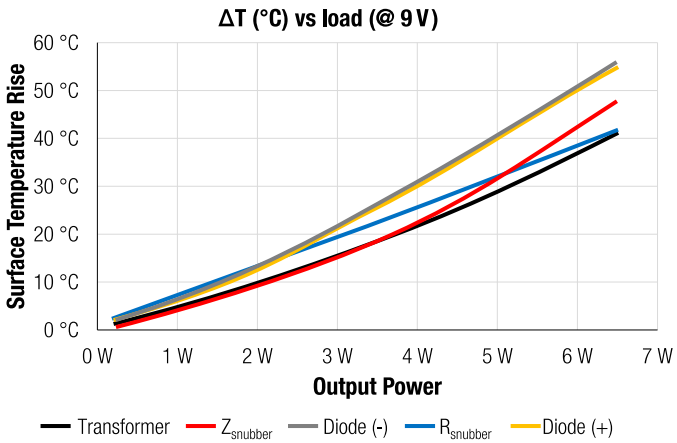


Figure 29: Temperature rise at V_{in} (min) = 9 V (worst-case)

Based on the above results, in order to keep internal/junction component temperatures within maximum ratings, it is recommended not to exceed a maximum ambient temperature of 80 °C (max) under operation for longer lifetime and higher reliability of the application.

If this ambient temperature is exceeded, the output power must be reduced (de-rated) accordingly.

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

10 EMC performance

EMC test results based on CISPR32-Class B limits are shown below for board variant-A. An input LC filter and a 10 cm x 10 cm copper plane connected to input GND equivalent to chassis as detailed below were added to pass the test. Operating conditions are V_{in} = 12 V with 6 W output resistive load (330 mA current draw per rail).

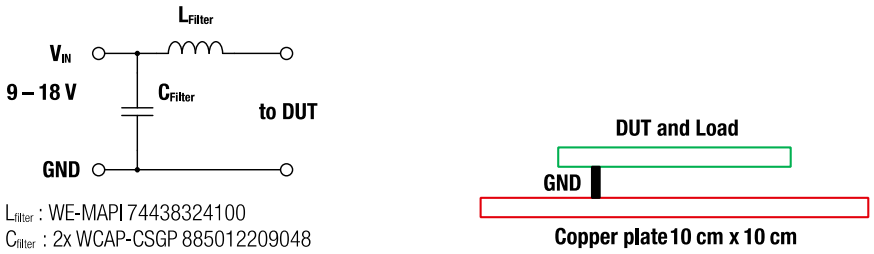


Figure 30: LC filter and copper plane added to pass CE and RE CISPR-32B EMC tests

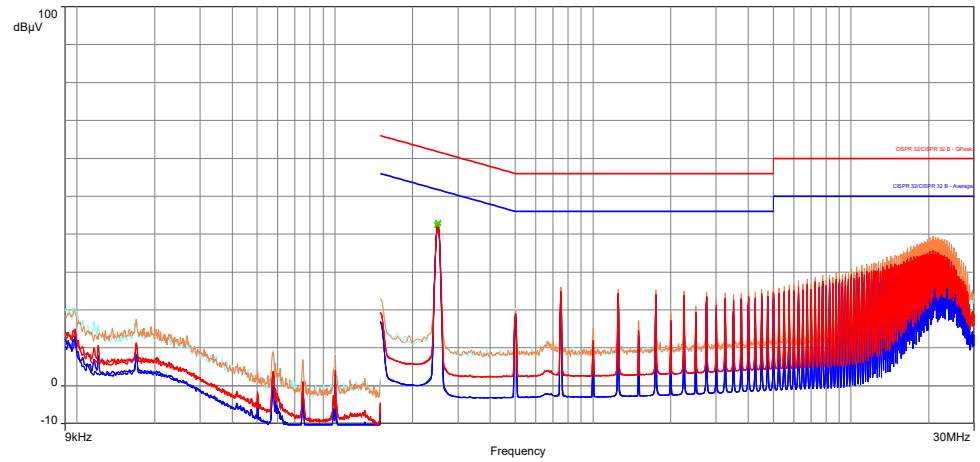


Figure 31: Conducted emissions results (CISPR32 class B limits)

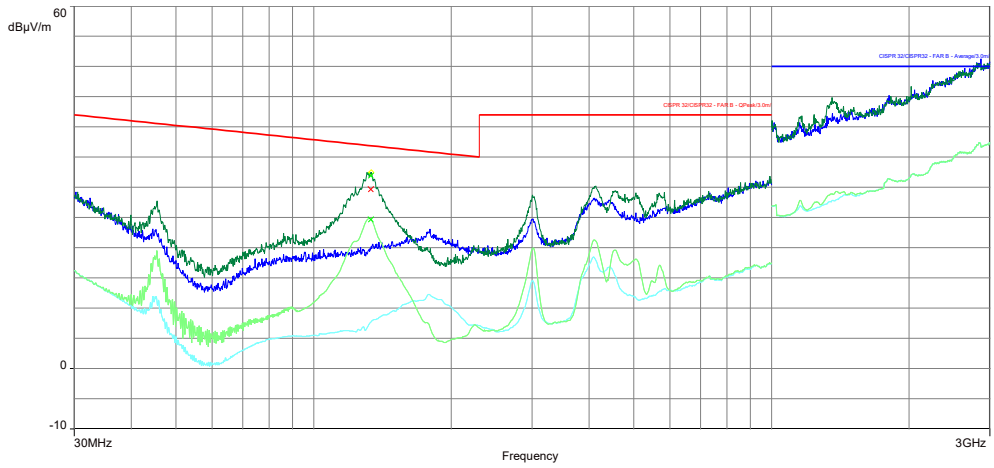


Figure 32: Radiated emissions results (CISPR32 class B limits) (30 cm length input cables)

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

11 Bill-of-Materials (BoM) Option 1: Standard

Reference designator	Description	Package	Manufacturer	MPN
C1, C2, C6, C7, C8	MLCC 10uF 50V X5R 10%	1206	Würth Elektronik	885012108022
C3, C4	MLCC 1uF 50V X7R 10%	0805	Würth Elektronik	885012207103
C5	MLCC 470pF 50V X7R 10%	0805	Würth Elektronik	885012207084
D1, D2, D3	Barrier Rectifier 1 A, 100 V	µSMP	Vishay	V1PM10-M3/H
D4	Zener 27 V, 0.5 W	µSMF	Vishay	BZD27C27P-M3
D5	Zener 16 V, 0.5 W	µSMF	Vishay	PLZ16B-G3/H
D6	Zener 4.8 V, 0.5 W	µSMF	Vishay	PLZ4V7B-G3/H
R1	Thick Film, 806k, 0.1 W, 1 %	0603	Yageo	RC0603FR-07806KL
R2	Thick Film, 232k, 0.1 W, 1 %	0603	Yageo	RC0603FR-07232KL
R3	Thin Film, 93.1k, 0.1 W, 0.1 %	0603	Yageo	RT0603BRD0793K1L
R4	Thin Film, 10k, 0.1 W, 0.1 %	0603	Yageo	RT0603BRD0710KL
R5 (DNP)	N/A	0603	N/A	N/A
R6	Thick Film, 100, 0.5 W, 5 %	0805	Bourns	CMP0805-FX-1000ELF
R7	Thick Film, 10k, 0.1 W, 1 %	0603	Yageo	RC0603FR-0710KL
R8	Thick Film, 3.3, 0.1 W, 1 %	0603	Yageo	RC0603FR-073R3L
Q1	MOSFET N-channel, 40 V	SOT23-3	Vishay	SQ2318AES-T1_BE3
U1	PSR Flyback Controller 65V 4.5A	SO-8	ADI / LT	LT8302HS8E#PBF
T1	Transformer dual-output 7uH, 4.5A, 7.5pF AEC-Q200	EP-7	Würth Elektronik	750318131

Table 3. Bill-of-Materials (BoM) Option 1: Standard

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

12 Bill-of-Materials (BoM) Option 2: AEC-Q qualified components

Reference designator	Description	Package	Manufacturer	MPN
C1, C2, C6, C7, C8	MLCC 10uF 50V X5R 10% AEC-Q200	1206	Murata	GRT31CR61H106KE01L
C3, C4	MLCC 1uF 50V CGJ 10% AEC-Q200	0805	TDK	CGJ4J3X7R1H105K125AB
C5	MLCC 470pF 50V X7R 10% AEC-Q200	0805	Kemet	C0805S471K5RACAUTO
D1, D2, D3	Barrier Rectifier 1 A, 100 V AEC-Q101	µSMP	Vishay	V1PM10HM3
D4	Zener 27 V, 0.5 W, AEC-Q101	µSMF	Vishay	BZD27C27P-HE3
D5	Zener 16 V, 0.5 W, AEC-Q101	µSMF	Vishay	PLZ16BHG3H
D6	Zener 4.8 V, 0.5 W, AEC-Q101	µSMF	Vishay	PLZ4V7BHG3H
R1	Thick Film, 806k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-07806KL
R2	Thick Film, 232k, 0.1 W, 1 %, AEC-Q101	0603	Yageo	AC0603FR-07232KL
R3	Thin Film, 93.1k, 0.1 W, 0.1 %, AEC-Q200	0603	Panasonic	ERA-3AEB9312V
R4	Thick Film, 10k, 0.1 W, 0.1 %, AEC-Q200	0603	Panasonic	ERA-3ARB103V
R5 (DNP)	N/A	0603	N/A	N/A
R6	Thick Film, 100, 0.5 W, 5 %, AEC-Q200	0805	Vishay	CRCW0805100RJNEAHP
R7	Thick Film, 10k, 0.1 W, 1 % AEC-Q200	0603	Yageo	AC0603FR-0710KL
R8	Thick Film, 3.3, 0.1 W, 1 % AEC-Q200	0603	Yageo	AC0603FR-073R3L
Q1	MOSFET N-channel, 40 V, AEC-Q101	SOT23-3	Vishay	SQ2318AES-T1_GE3
U1	PSR Flyback Controller 65V 4.5A AEC-Q200	SO-8	ADI / LT	LT8302HS8E#WPBF
T1	Transformer dual-output 7uH, 4.5A, 7.5pF AEC-Q200	EP-7	Würth Elektronik	750318131

Table 4: Bill-of-Materials (BoM), option 2: AEC-Q qualified components

Reference Design

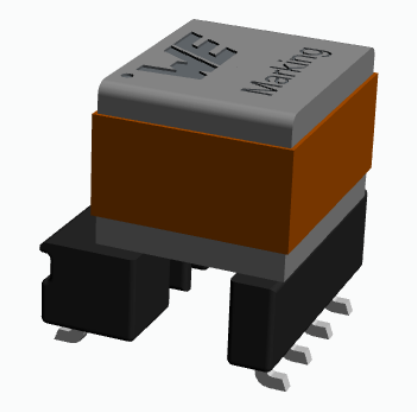
6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

13 WE-AGDT series

The WE-AGDT (Auxiliary Gate Drive Transformer) series from Würth Elektronik include six transformers, all using a compact EP7 assembly and each optimized for its corresponding reference design. They provide bipolar (+15 V; -4 V) as well as unipolar (15 to 20 V; 0 V) options, with input voltage ranging from 9 to 36 V and maximum output power of 3 to 6 W. They are optimized for SiC applications, but they are also suitable for driving IGBT and power MOSFETs alike, and even high-voltage GaN-FETs with the correct output regulation stage.

Characteristics

- Interwinding capacitance as low as 6.8 pF typical
- Flyback with primary side regulation
- High efficiency and very compact. Surface mount EP7
- Common control voltages for SiC MOSFET
- Wide range input voltages 9 to 36 V
- Safety: IEC62368-1 /IEC61558-2-16
- Basic insulation
- Dielectric insulation up to 4 kV
- Temperature class B
- Reference designs with TI and ADI



Applications

Industrial drives, AC motor inverters, electric vehicle powertrain, battery chargers, solar inverters, data centers, uninterruptible power supplies, active power factor correction, switching power supplies with SiC-MOSFETs.

Order code	V_{in} range (V)	V_{out1} (V)	V_{out2} (V)	C_{w_w} (pF)	Frequency max (kHz)	IC Reference Design	Power (W)
750317893	9 – 18	15 – 20	-	6.8	350	LM5180	3
750317894	9 – 18	15	-4	7.5			
750318207	18 – 36	15 – 20	-	8.2			5
750318208	18 – 36	15	-4	7.0			
750318114	9 – 18	15 – 20	-	6.8		LT8302	6
750318131	9 – 18	15	-4	6.8			

Table 5: WE-AGDT transformer series

Reference Design

6 W Isolated bipolar auxiliary power supply for SiC-MOSFET gate driver

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