# A Seven-Nanosecond Comparator for Single Supply Operation

## Guidance for Putting Civilized Speed to Work

Jim Williams

## INTRODUCTION

In 1985 Linear Technology Corporation introduced the LT®1016 Comparator. This device was the first readily usable, high speed TTL comparator. Previous ICs were either too slow or unstable, preventing widespread acceptance. The LT1016 was, and is, a highly successful product.

Recent technology trends have emphasized low power, single supply operation. The LT1016, although capable of such operation, does not include ground in its input range. As such, it must be biased into its operating common mode range for practical single supply use. A new device, the LT1394, maintains the speed and application civility of its predecessor while including ground in its input operating range. Additionally, the new comparator is faster and pulls significantly lower operating current than the LT1016.

This publication borrows shamelessly from earlier LTC efforts, while introducing new material.[1] It approximates, affixes, appends, abridges, amends, abbreviates, abrogates, ameliorates and augments the previous work.[2] More specifically, the applications section has been almost entirely refurbished, reflecting the LT1394's single supply agility. Additionally, tutorial content has been expanded beyond previous efforts. This approach is necessitated by the continuing need for tutorial guidance in the application of high speed linear devices. The rules of the game are never obviated by new components; rather, they become even more significant as performance increases.

Comparators may be the most underrated and underutilized monolithic linear component. This is unfortunate because comparators are one of the most flexible and universally applicable components available. In large measure the lack of recognition is due to the IC op amp, whose versatility allows it to dominate the analog design world. Comparators are frequently perceived as devices that crudely express analog signals in digital form—a 1-bit A/D converter. Strictly speaking, this viewpoint is correct. It is also wastefully constrictive in its outlook. Comparators don't "just compare" in the same way that op amps don't "just amplify."

Comparators, in particular high speed comparators, can be used to implement linear circuit functions which are as sophisticated as any op amp-based circuit. Judiciously combining a fast comparator with op amps is a key to achieving high performance results. In general, op amp-based circuits capitalize on their ability to close a feedback loop with precision. Ideally, such loops are maintained continuously over time. Conversely, comparator circuits are often based on speed and have a discontinuous output over time. While each approach has its merits, a fusion of both yields the best circuits.

This effort's initial sections are devoted to familiarizing the reader with the realities and difficulties of high speed

**Note 1:** In particular LTC Application Note 13, "High Speed Comparator Techniques." Additional text has been similarly purloined from other LTC sources. See the References section following the main text for specifics.
**Note 2:** An alliterative amalgamated assemblage.

comparator circuit work. The mechanics and subtleties of achieving precision circuit operation at DC and low frequency have been well documented. Relatively little has appeared that discusses, in practical terms, how to get fast circuitry to work. In developing such circuits, even the most veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high speed circuits can only work if negotiated compromises with nature are arranged. Ignorance of, or contempt for, physical law is a direct route to frustration. In this regard, much of the text and appendices are directed at developing awareness of, and respect for, circuit parasitics and fundamental limitations. This approach is maintained in the applications section, where the notion of "negotiated compromises" is expressed in terms of resistor values and compensation techniques. Many of the application circuits use the LT1394's speed to improve on a standard circuit. Some utilize the speed to implement a traditional function in a nontraditional way, with attendant advantages. A (very) few operate at or near the state-of-the-art for a given circuit type, regardless of approach. Substantial effort has been expended in developing these examples and documenting their operation. The resultant level of detail is justified in the hope that it will be catalytic. The circuits should stimulate new ideas to suit particular needs, while demonstrating the LT1394's capabilities in an instructive manner.

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## THE LT1394 — AN OVERVIEW

A new ultrahigh speed comparator, the LT1394, features TTL-compatible complementary outputs and 7ns response time. Other capabilities include a latch pin and good DC input characteristics (see Figure 1). The LT1394's outputs directly drive all 5V families, including the higher speed ASTTL, FAST and HC parts. Additionally, TTL outputs make the device easier to use in linear circuit applications where ECL output levels are often inconvenient.

A substantial amount of design effort has made the LT1394 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1394 is stable in its linear region. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. Finally, current consumption is far lower than previous devices. These features make the 200GHz gain bandwidth LT1394 considerably easier to apply than other fast comparators. Unfortunately, laws of physics dictate that the circuit *environment* the LT1394 works in must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance and layout. Some of these considerations are present in digital systems, where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1394 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1394's (Trace B) response to the pulse generator (Trace A) is faster than a TTL inverter (Trace C)! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

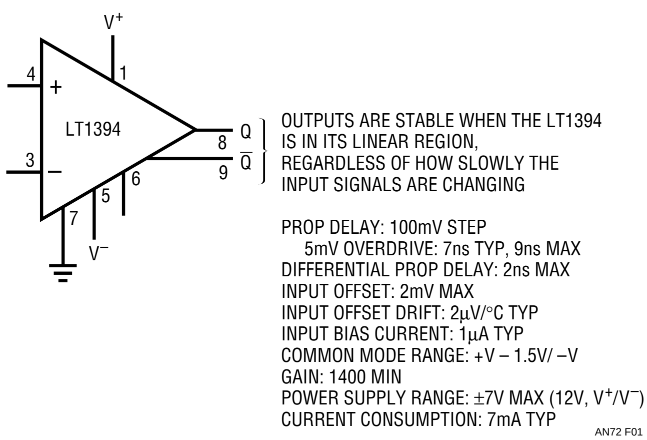


**Figure 1. The LT1394 at a Glance**

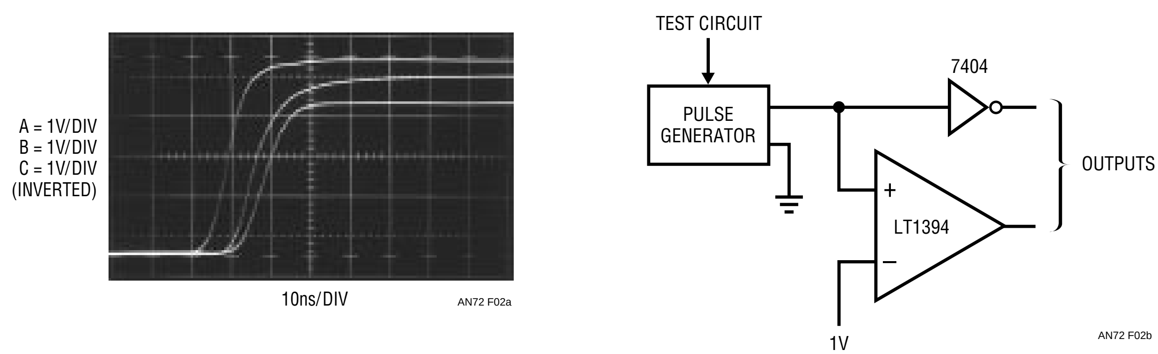


**Figure 2. LT1394 vs a TTL Gate**

## The Rogue's Gallery of High Speed Comparator Problems

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully (see "About Bypass Capacitors" in the Tutorial section). An unbypassed LT1394 is shown responding to a pulse input in Figure 3. The power supply the LT1394 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1394, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. Although the LT1394 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors*.

In Figure 4 the LT1394's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount them as close as possible to the LT1394. An inch of wire between the capacitor and the LT1394 can cause problems*.

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V—quite a trick for a device running from a 5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes that match your oscilloscope's input characteristics and compensate them properly* (for a discussion on probes, see "About Probes and Probing Techniques" in the Tutorial section). Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 7ns response time LT1394 appears to have 50ns edges! In this case, the probe used is too heavily compensated or slow for the oscilloscope.

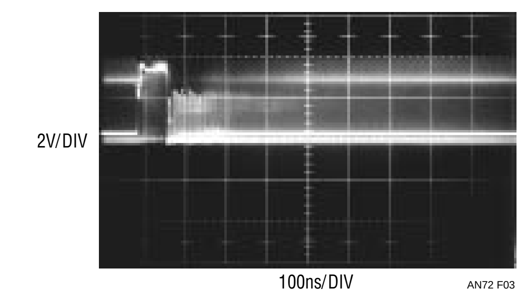


**Figure 3. Unbypassed LT1394 Response**

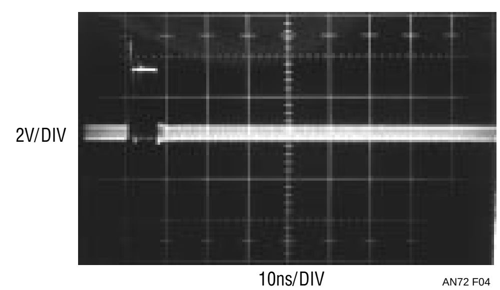


**Figure 4. LT1394 Response with Poor Bypassing**

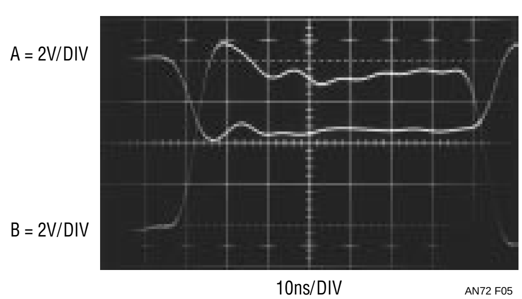


**Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error**

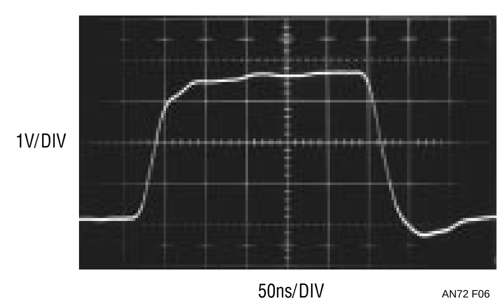


**Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow**

Never use 1× or “straight” probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure that it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

In Figure 7 the probes are properly selected and applied but the LT1394’s output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about six inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips that fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed one inch in length. *Keep the probe ground connection as short as possible*.

The difficulty in Figure 8 is delay and inadequate amplitude (Trace B). A small delay on the leading edge is followed by a large delay before the falling edge begins. Additionally, a lengthy, tailing response stretches 70ns before finally settling out. The amplitude only rises to 1.5V. A common oversight is responsible for these conditions.

A FET probe monitors the LT1394 output in this example. The probe’s common mode input range has been exceeded, causing it to overload and clip the output badly. The small delay on the rising edge is characteristic of active probes and is legitimate. During the time the output is high, the probe is driven deeply into saturation. When the output falls, the probe’s overload recovery is lengthy and uneven, causing the delay and tailing.

*Know your FET probe. Account for the delay of its active circuitry. Avoid saturation effects due to common mode input limitations (typically ±1V). Use 10× and 100× attenuator heads when required*.

Figure 9 shows the LT1394’s output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1394’s ground pin connection is one inch long. The ground lead of the LT1394 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1394’s ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1394’s ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets*.

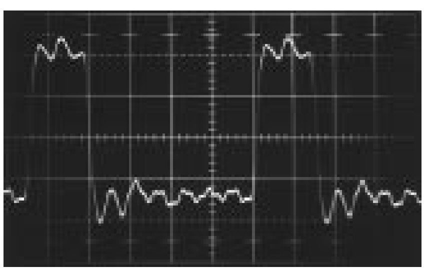


**Figure 7. Typical Results Due to Poor Probe Grounding**

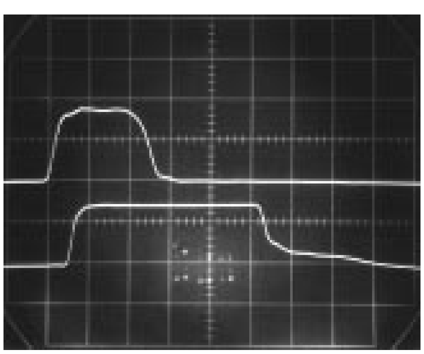


**Figure 8. Overdriven FET Probe Causes Delayed, Tailing Response**

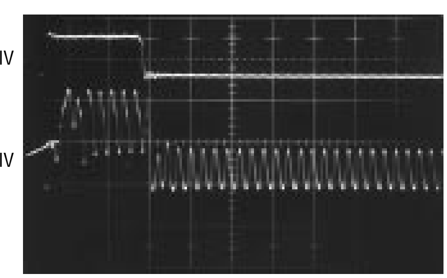


**Figure 9. Excessive LT1394 Ground Path Resistance Causes Oscillation**

Figure 10 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1394 without a "ground plane." A ground plane is formed by using a continuous conductive plane over the surface of the circuit board (ground plane theory is discussed in the Tutorial section). The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1394.*

"Fuzz" on the edges is the difficulty in Figure 11. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3kΩ input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedance as low as possible, preferably 1kΩ or less. Route output and input pins and components away from each other.*

The opposite of stray-caused oscillations appears in Figure 12. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input and output delay occurs. An RC combination of 2kΩ source resistance and 10pF to ground gives a 20ns time constant—significantly longer than the LT1394's response time. *Keep source impedance low and minimize stray input capacitance to ground.*

Figure 13 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be cause by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few circumstances

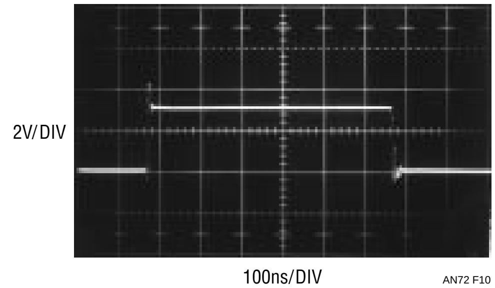


**Figure 10. Transition Instabilities Due to No Ground Plane**

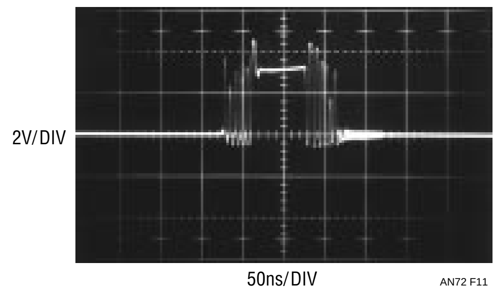


**Figure 11. 3pF Stray Capacitive Feedback with 3kΩ Source Can Cause Oscillation**

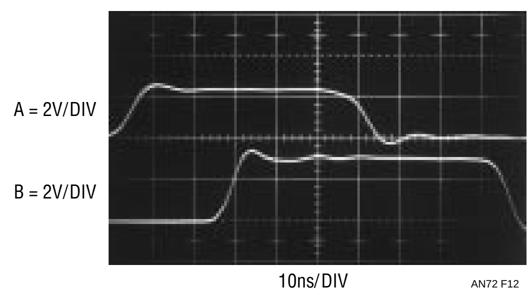


**Figure 12. Stray 5pF Capacitance from Input to Ground Causes Delay**

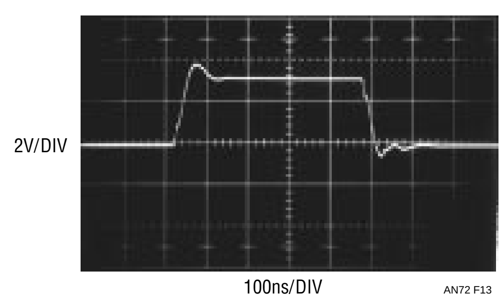


**Figure 13. Excessive Load Capacitance Forces Edge Distortion**

it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load*.

Another output-caused fault is shown in Figure 14. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead that is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. Similarly, outputs and inputs can see excursions outside supply bounds due to poorly terminated lines, causing device misfunction or failure. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω to 400Ω). Ensure that device terminals remain inside supply limits at all times*.

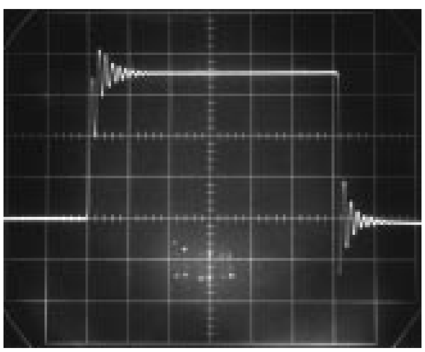


**Figure 14. Lengthy, Unterminated Output Lines Ring from Reflections**

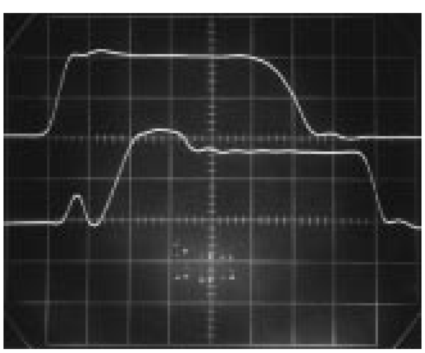


**Figure 15. Input Common Mode Overdrive Generates Odd Outputs**

A final malady is presented in Figure 15. These waveforms are reminiscent of Figure 12's input RC-induced delay. The output waveform initially responds to the input's leading edge, but then returns to zero before going high again. When it does go high, it slews slowly. Additional odd characteristics include pronounced overshoot and pulse top aberration. The fall time is also slow and well delayed from the input. This is certainly strange behavior from a TTL output. What is going on here? The input pulse is responsible for all these anomalies. Its 10V amplitude is well outside the 5V-powered LT1394's common mode input range. Internal input clamps prevent this pulse from damaging the LT1394, but an overdrive of this magnitude results in poor response. *Keep input signals inside the LT1394's common mode range at all times*.

## TUTORIAL SECTION

An implied responsibility in raising the aforementioned issues is their solution or elimination. What good is all the rabble-rousing without suggestions for fixes? It is in this spirit that this tutorial section is presented. Theory, techniques, prejudice and just plain gossip are offered as tools that may help avoid or deal with difficulties.

### About Pulse Generators

A significant consideration for fast comparator development work is the pulse generator. Features such as variable rise and fall time, output DC biasing capability, triggering facilities and amplitude range are highly desirable. General purpose pulse generators usually provide some or all of these capabilities, and little editorial comment is required. Less common, however, particularly at any reasonable price, are really fast pulse generators suitable for LT1394 work. Relatively few generators have transition times below 2.5ns. This kind of speed is highly desirable and some noteworthy instruments bear mention.

The current production Hewlett-Packard 8110A has a fairly complete set of features and 2ns transition times, and is typical of modern, high speed instruments. The older HP-8082A is more versatile, has clean subnanosecond transitions and the "knob driven" panel controls are intuitively easy to use. The Phillips PM-5771, also well endowed with features, has 2.4ns transitions and is quite inexpensive. Finally, the HP215A, long out of manufacture, is a special case. This instrument has a restricted 0 to 100ns width range and no rise time control, but other features make it uniquely useful. The output has subnanosecond transitions with extraordinarily well-controlled and specified pulse shape parameters. The trigger is very agile, permitting continuous time phase adjustment from before to after the main output. External trigger impedance, polarity and sensitivity are also variable. The output, controlled by a stepped attenuator, will put ±10V into 50Ω in 800ps.

In general, select a pulse generator with the features needed for the circuit of interest. Also, take the time to acquaint yourself with output pulse characteristics, particularly at the highest speeds. Finally, (this is unadulterated author prejudice), instruments with knobs remain easier and faster to set up and modify than "menu-driven" types. This is important in bench work where the ability to quickly and easily change instrument operating point is paramount. In this regard knobs have no equal. Menus belong in restaurants.

### About Cables, Connectors and Terminations

High speed signals should always be routed to and from the circuit board with good quality coaxial cable. The cable should be driven and terminated in the system's characteristic impedance at the drive and load points. The driven end is usually an instrument (e.g., pulse or signal generator), presumably endowed with proper characteristics by its manufacturer. It is the cable and its termination, selected by the experimenter, that often cause problems.

All coaxial cable is not the same. Use cable appropriate to the system's characteristic impedance and of good quality. Poorly chosen cable materials or construction methods can introduce odd effects at very high speeds, resulting in observed waveform distortion. A poor cable choice can adversely affect 0.01% settling in the 100ns to 200ns region. Similarly, poor cable can preclude maintenance of even the cleanest pulse generator's 1ns rise time or purity. Typically, inappropriate cable can introduce tailing, rise time degradation, aberrations following transitions, nonlinear impedance and other undesirable characteristics.

Termination choice is equally important. Good quality BNC coaxial type terminators are usually the best choice for breadboarding. Their impedance vs frequency is flat into the GHz range. Additionally, their construction ensures that the (often substantial) drive current returns directly to the source, instead of being dumped into the breadboard's ground system. BNC coaxial terminators are not simply resistors in a can. Good grade 50Ω terminators maintain true coaxial form. They use a carefully designed 50Ω resistor with significant effort devoted to connections to the actual resistive element. In particular, the largest possible connection surface area is utilized to minimize high speed losses. These construction techniques ensure optimum wideband response. Figures 16 and 17 demonstrate this nicely. In Figure 16 a 1ns pulse with 350ps rise and fall times[3] is monitored on a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling

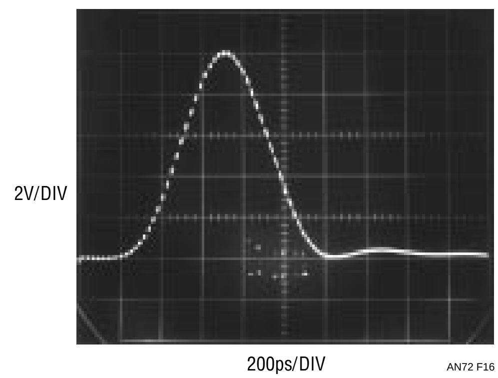


**Figure 16. 350ps Rise and Fall Times Are Preserved by a Good Quality Termination**

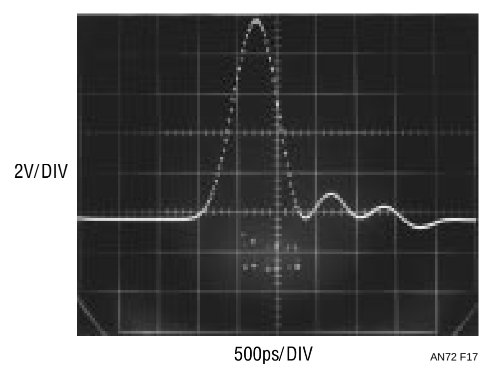


**Figure 17. Poor Grade Termination Produces Pronounced Ringing and Tailing in the GHz Range**

**Note 3:** The ability to generate such a pulse proves useful for a variety of tasks, including testing terminators, cables, probes and oscilloscopes for response. The requirements for this pulse generator are surprisingly convenient and inexpensive. For a discussion and construction details see Appendix B "Measuring Probe-Oscilloscope Response."

plug-in and P6032 probe). The waveform is clean, with only a slight hint of ring after the falling edge. This photo was taken with a high grade BNC coaxial type terminator in use. Figure 17 does not share these attributes. Here, the generator is terminated with a 50Ω carbon composition resistor with lead lengths of about 1/8 inch. The waveform rings and tails badly on turn-off before finally settling. Note that the sweep speed required a 2.5× reduction to capture these unwanted events. Variable attenuators must provide performance similar to fixed types for meaningful results. The HP-355 series are excellent units, with high fidelity response to 1GHz.

Connectors, such as BNC barrel extensions and tee-type adaptors, are convenient and frequently employed. Remember that these devices represent a discontinuity in the cable, and can introduce small but undesirable effects. In general it is best to employ them as close as possible to a terminated point in the system. Use in the middle of a cable run provides minimal absorption of their mismatch and reflections. The worst offenders among connectors are adapters. This is unfortunate, as these devices are necessitated by the lack of connection standardization in wideband instrumentation. The mismatch caused by a BNC-to-GR874 adaptor transition at the input of a wideband sampling 'scope is small, but clearly discernible in the display. Similarly, mismatches in almost all adaptors, and even in "identical" adaptors of different manufacture, are readily measured on a high frequency network analyzer such as the Hewlett-Packard 4195A[4] (for additional wisdom and terror along these lines see Reference 1).

BNC connections are easily the most common, but not necessarily the most desirable, wideband connection mechanism. The ingenious GR874 connector has notably superior high frequency characteristics, as does the type N. Unfortunately, it's a BNC world out there.

### About Probes and Probing Techniques

The choice of which oscilloscope probe to use in a measurement is absolutely crucial. The probe must be considered as an inherent part of the circuit under test. Rise time, bandwidth, resistive and capacitive loading, delay and other limitations must be kept in mind.

Sometimes, the best probe is no probe at all. In some circumstances it is possible and preferable to connect critical breadboard points *directly* to the oscilloscope (see Figure 18). This arrangement provides the highest possible grounding integrity, eliminates probe attenuation, and maintains bandwidth. In most cases this is mechanically inconvenient, and often the oscilloscope's electrical characteristics (particularly input capacitance) will not permit it. This is why oscilloscope probes were developed, and why so much effort has been put into their development (Reference 11 is excellent).

Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the point they are measuring. The most obvious is input resistance, but input capacitance usually dominates in a high speed measurement. Much time can be lost chasing circuit events that are actually due to improperly selected or applied probes. An 8pF probe looking at a 1kΩ source impedance forms an 8ns lag— longer than the LT1394's delay time! Pay particular attention to the probe's input capacitance. Standard 10MΩ, 10× probes typically have 8pF to 10pF of input capacitance, with 1× types being much higher. In general, 1× probes are not suitable for fast work because their bandwidth is limited to about 20MHz. Remember that all 10× probes cannot be used with all oscilloscopes; the probe's compensation range must match the oscilloscope's input capacitance. Low impedance probes (with 500Ω to 5kΩ resistance) designed for 50Ω inputs, usually have input capacitance of 1pF or 2pF. They are a very good choice if you can stand the low resistance. FET probes maintain high input resistance and keep capacitance at the 1pF level but have substantially more delay than passive probes. FET probes also have limitations on input common mode range which must be adhered to or serious measurement errors will result. Contrary to popular belief, FET probes *do not* have extremely high input resistance—some types are as low as 100kΩ.

Regardless of which type probe is selected, remember that they all have bandwidth and rise time restrictions. The displayed rise time on the oscilloscope is the vector sum of source, probe and 'scope rise times.

$$t_{RISE} = \sqrt{(t_{RISE}\text{ Source})^2 + (t_{RISE}\text{ Probe})^2 + (t_{RISE}\text{ Oscilloscope})^2}$$

This equation warns that some rise time degradation must occur in a cascaded system. In particular, if probe and

**Note 4:** Almost no one believes any of this until they see it for themselves. I didn't. Photos of the network analyzer's display aren't included in the text because no one would believe them. I wouldn't.

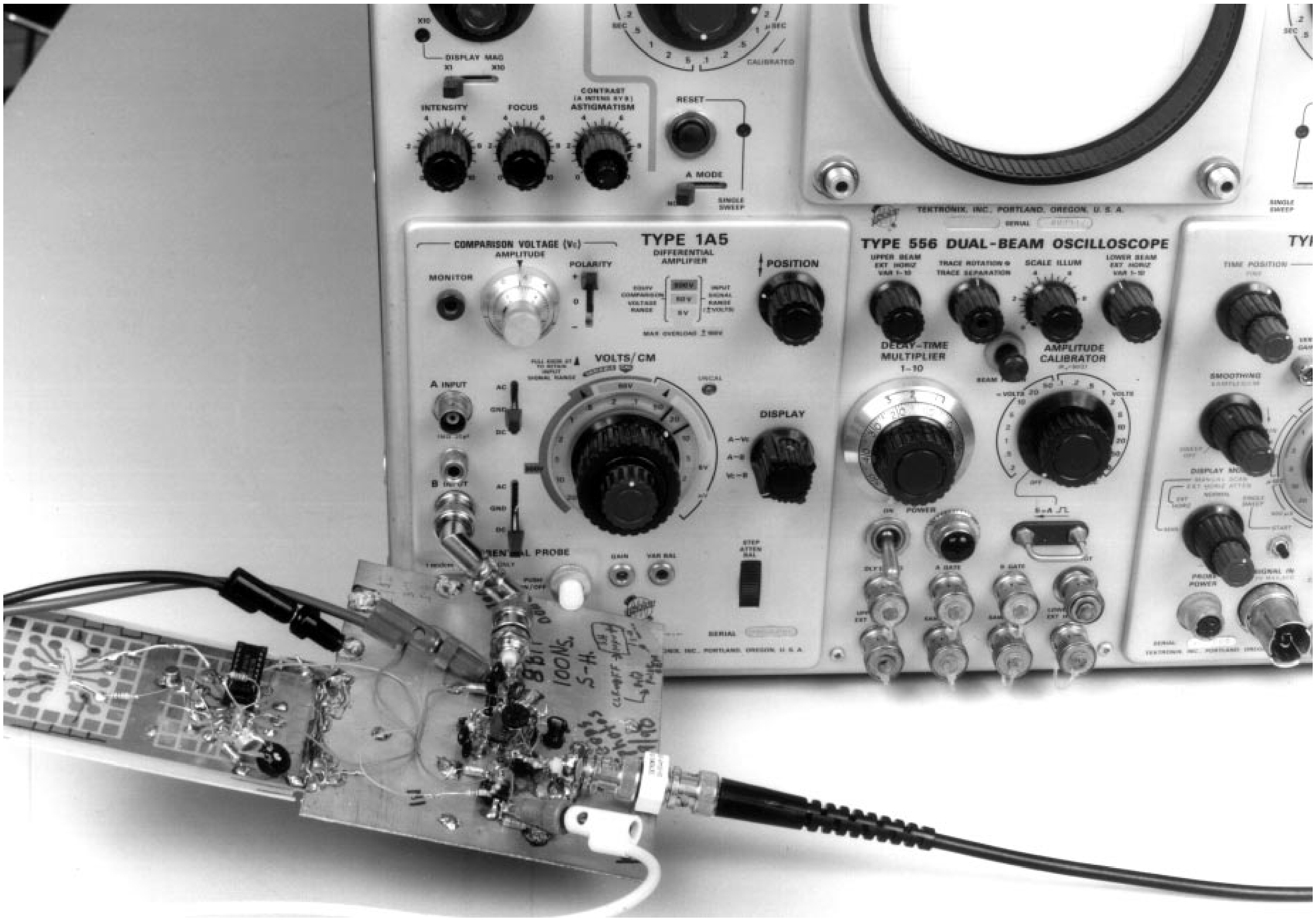


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**Figure 18. Sometimes the Best Probe Is No Probe. Direct Connection to the Oscilloscope Eliminates a 10× Probe's Attenuation and Possible Grounding Problems**

oscilloscope are rated at the same rise time, the system response will be slower than either.

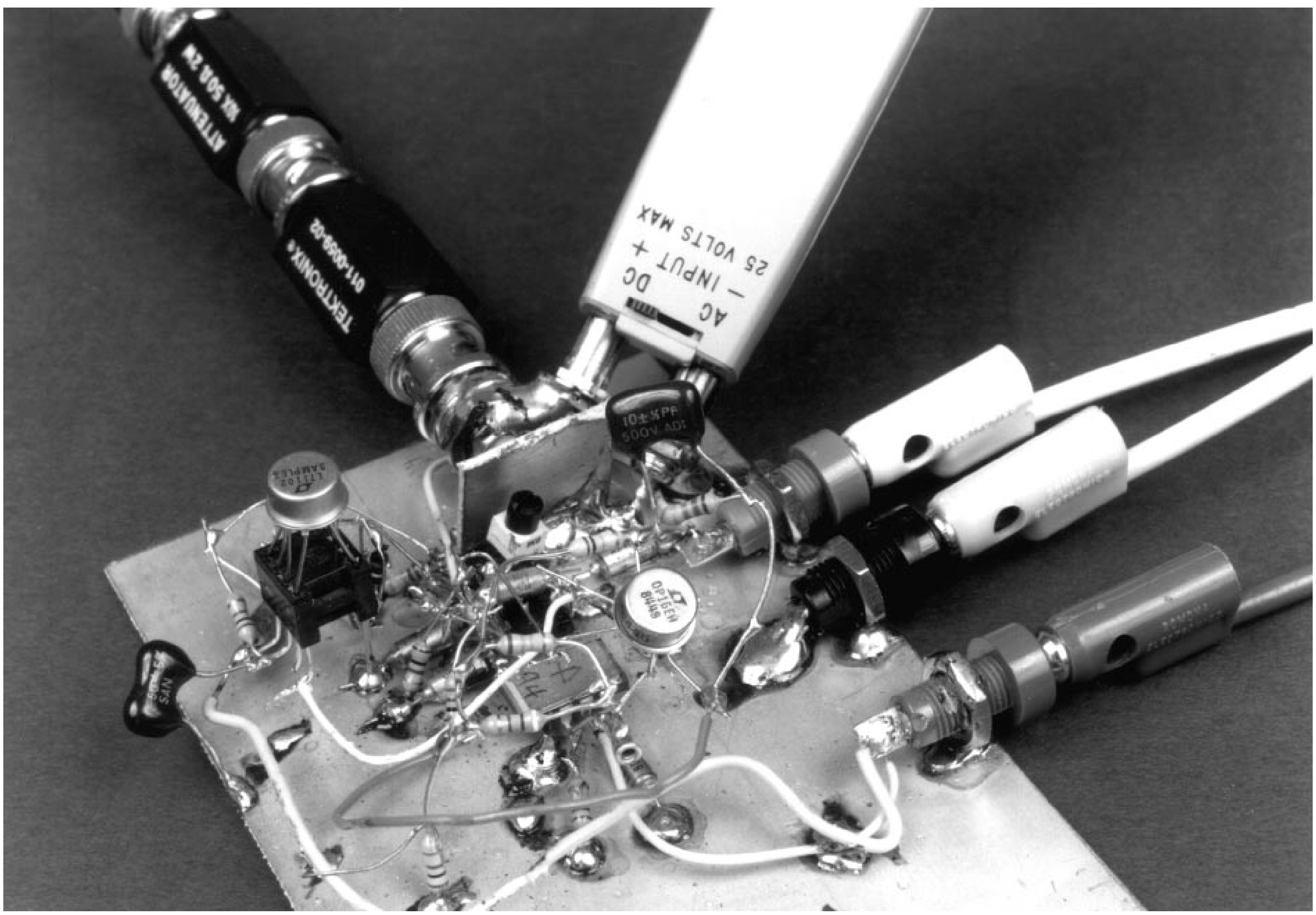
Current probes are useful and convenient.[5] The passive transformer-based types are fast and have less delay than the Hall effect stabilized versions. The Hall types, however, respond at DC and low frequency and the transformer types typically roll off around 100Hz to 1kHz. Both types have saturation limitations, which, when exceeded, cause odd results on the CRT, confusing the unwary. The Tektronix type CT-1 current probe, although not nearly as versatile as the clip-on probes, bears mention. Although this is not a clip-on device, it may be the least electrically intrusive way of extracting wideband signal information. Rated at 1GHz bandwidth, it produces 5mV/mA output with only 0.6pF loading. Decay time constant of this AC current probe is ≈1%/50ns, resulting in a low frequency limit of 35kHz.

A very special probe is the differential probe. A differential probe may be thought of as two matched FET probes contained within a common probe housing. This probe literally brings the advantage of a differential input oscilloscope to the circuit board. The probes matched, active circuitry provides greatly improved high frequency common mode rejection over single-ended probing or even matched passive probes used with a differential amplifier. The resultant ability to reject common mode signals and ground noise at high frequency allows this probe to deliver exceptionally clean results when monitoring small, fast signals. Figure 19 shows a differential probe being used to verify the waveshape of a 2.5mV circuit input.

**Note 5:** A more thorough discussion of current probes is given in LTC Application Note 35, "Step-Down Switching Regulators." See Reference 2.

When using different probes, remember that they all have different delay times, meaning that apparent timing errors will occur on the CRT. Know what the individual probe delays are and account for them in interpreting the CRT display.

By far the greatest source of error in probe use is grounding. Poor probe grounding can cause ripples and discontinuities in the observed waveform. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is parasitic inductance in the probe's ground connection. In most oscilloscope measurements this is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in making the lowest possible inductive connection to ground. Most of these attachments assume a ground plane is in use, which it should be. Always try to make the shortest possible connection to ground—anything longer than one inch may cause trouble. Sometimes it's difficult to determine if probe grounding is the cause of observed waveform aberrations. One good test is to disturb the grounding setup and see if changes occur. Nominally, touching the ground plane or jiggling probe ground connectors or wires should have no effect. If a ground strap wire is in use try changing its orientation or simply squeezing it together to change and minimize its loop area. *If any waveform change occurs while doing this the probe grounding is unacceptable, rendering the oscilloscope display unreliable.*




AN72 F19

**Figure 19. Using a Differential Probe to Verify the Integrity of a 2.5mV High Speed Input Pulse**

The simple network of Figure 20 shows just how easy it is for poorly chosen or used probes to cause bad results. A 9pF input capacitance probe with a 4-inch long ground strap monitors the output (Trace B, Figure 21). Although the input (Trace A) is clean, the output contains ringing. Using the same probe with a 1/4-inch spring tip ground connection accessory seemingly cleans up everything (Figure 22). However, substituting a 1pF FET probe (Figure 23) reveals a 50% output amplitude error in Figure 22! The FET probe's low input capacitance allows a more accurate version of circuit action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5ns due to delay in its active circuitry. Hence, separate measurements with each probe are required to determine the output's amplitude and timing parameters. An alternative would employ two matched FET probes to minimize delay uncertainty.

A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can be used to introduce stray capacitance to a suspected circuit node while observing results on the CRT. Two fingers, lightly moistened, can be used to provide an experimental resistance path. Some high speed engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

Examples of some of the probes discussed, along with different forms of grounding implements, are shown in Figure 24. Probes A, B, E and F are standard types equipped with various forms of low impedance grounding attachments. The conventional ground lead used on G is more convenient to work with but will cause ringing and other effects at high frequencies, rendering it useless. H

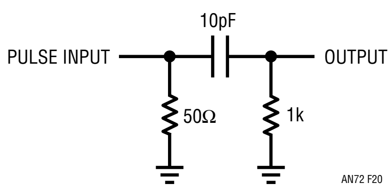



**Figure 20. Probe Test Circuit**

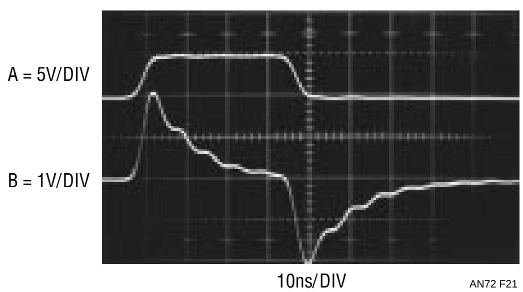



**Figure 21. Test Circuit Output with 9pF Probe and 4-Inch Ground Strap**

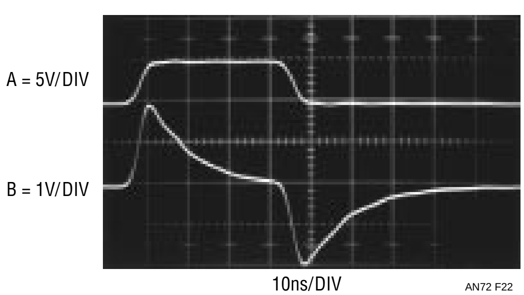



**Figure 22. Test Circuit Output with 9pF Probe and 1/4-Inch Ground Strap**

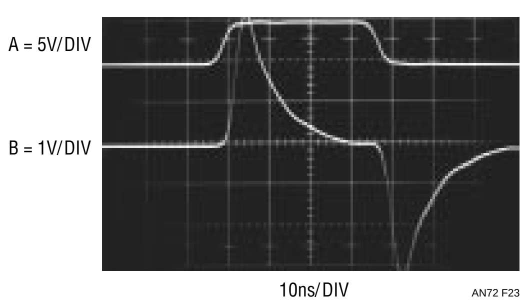



**Figure 23. Test Circuit Output with FET Probe**

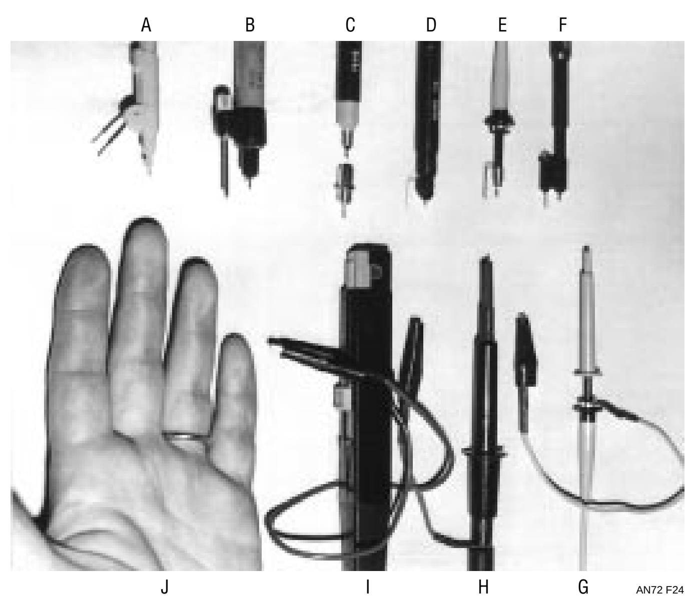



**Figure 24. Various Probe-Ground Strap Configurations**

has a very short ground lead. This is better, but can still cause trouble at high speeds. D is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. C is a separated FET probe attenuator head. Such heads allow the probe to be used at higher voltage levels (e.g., ±10V or ±100V). The miniature coaxial connector shown can be mounted on the circuit board and the probe mated with it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended. I is a current probe. A ground connection is not usually required. However, at high speeds the ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible. J is typical of the finger probes described in the text. Note the ground strap on the third finger.

The low inductance ground connectors shown are available from probe manufacturers and are always supplied with good quality, high frequency probes. Because most oscilloscope measurements do not require them, they invariably become lost. There is no substitute for these devices when they are needed, so it is prudent to take care of them. This is especially applicable to the ground strap on the finger probe.

**About Oscilloscopes**

The modern oscilloscope is one of the most remarkable instruments ever constructed. The protracted and intense development effort put toward these machines is perhaps equaled only by the fanaticism devoted to timekeeping.[6] It is a tribute to oscilloscope designers that instruments manufactured over 30 years ago still suffice for over 90% of today's measurements. The oscilloscope-probe combination used in high speed work is the most important equipment decision the designer must make. Ideally, the oscilloscope should have at least 150MHz bandwidth, but slower instruments are acceptable if their limitations are well understood. Be certain of the characteristics of the probe-oscilloscope combination. Rise time, bandwidth, resistive and capacitive loading, delay, noise, channel-to-channel feedthrough, overdrive recovery, sweep nonlinearity, triggering, accuracy and other limitations must be kept in mind. High speed linear circuitry demands a great deal from test equipment and countless hours can be saved if the characteristics of the instruments used are well known. Obscene amounts of time have been lost pursuing "circuit problems" that in reality are caused by misunderstood, misapplied or out-of-spec equipment. Intimate familiarity with your oscilloscope is invaluable in getting the best possible results with it. In fact, it is possible to use seemingly inadequate equipment to get good results if the equipment's limitations are well known and respected. All of the circuits in the Applications section involve rise times and delays well above the 100MHz to 200MHz region, but 90% of the development work was done with a 50MHz oscilloscope. Familiarity with equipment and thoughtful measurement technique permit useful measurements seemingly beyond instrument specifications. A 50MHz oscilloscope cannot track a 5ns rise time pulse, but it can measure a 2ns delay between two such events. Using such techniques, it is often possible to deduce the desired information. There are situations where no amount of cleverness will work and the right equipment (e.g., a faster oscilloscope) must be used. Sometimes, "sanity-checking" a limited bandwidth instrument with a higher bandwidth oscilloscope is all that is required. For high speed work, brute force bandwidth is indispensable when needed, and no amount of features or computational sophistication will substitute. Most high speed circuitry does not require more than two traces to get where you are going. Versatility and many channels are desirable, but if the budget is limited, spend for bandwidth!

Dramatic differences in displayed results are produced by probe-oscilloscope combinations of varying bandwidths. Figure 25 shows the output of a very fast pulse[7] monitored with a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in). At this bandwidth the 10V amplitude appears clean, with just a small hint of ringing after the falling edge. The rise and fall times of 350ps are suspicious, as the sampling oscilloscope's rise time is also specified at 350ps.[8]

**Note 6:** In particular, the marine chronometer received ferocious and abundant amounts of attention. See References 4, 5 and 6. For an enjoyable stroll through the history of oscilloscope vertical amplifiers, see Reference 3.

**Note 7:** See Appendix B "Measuring Probe-Oscilloscope Response," for complete details on this pulse generator.

**Note 8:** This sequence of photos was shot in my home lab. I'm sorry, but 1GHz was the fastest 'scope in my house at the time. See Appendix B for a higher speed representation of this pulse.

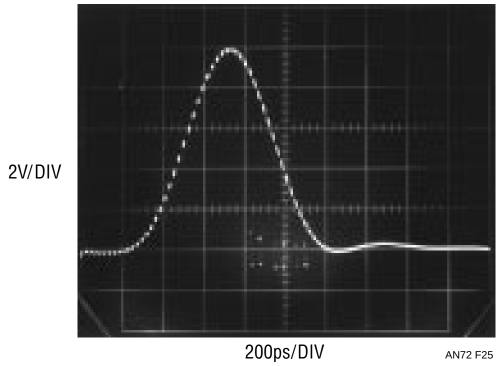



**Figure 25. A 350ps Rise/Fall Time 10V Pulse Monitored on 1GHz Sampling Oscilloscope. Direct 50Ω Input Connection Is Used**

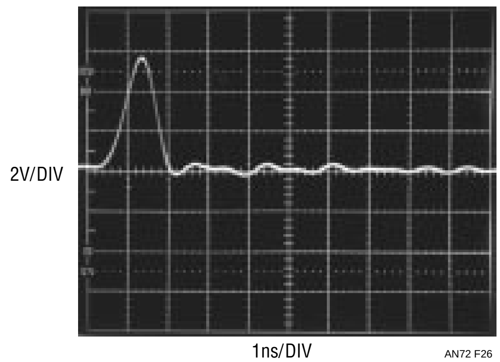



**Figure 26. The Test Pulse Appears Smaller and Slower on a 350MHz Instrument ($t_{RISE}$ = 1ns). Deliberate Poor Grounding Creates Rippling After the Pulse Falls. Direct 50Ω Connection Is Used**

Figure 26 shows the same pulse observed on a 350MHz instrument with a direct connection to the input (Tektronix 485/50Ω input). Indicated rise time balloons to 1ns, while displayed amplitude shrinks to 6V, reflecting this instrument’s lesser bandwidth. To underscore earlier discussion, poor grounding technique ( 1 1/2" of ground lead to the ground plane) created the prolonged rippling after the pulse fall.

Figure 27 shows the same 350MHz (50Ω input) oscilloscope with a 3GHz 10× probe (Tektronix P6056). Displayed results are nearly identical, as the probe’s high bandwidth contributes no degradation. Again, deliberate poor grounding causes overshoot and rippling on the pulse fall.

Figure 28 equips the same oscilloscope with a 10× probe specified at 290MHz bandwidth (Tektronix P6047). Additionally, the oscilloscope has been switched to its 1MΩ input mode, reducing bandwidth to a specified 250MHz. Amplitude degrades to less than 4V and edge times similarly increase. The deliberate poor grounding contributes the undershoot and underdamped recovery on pulse fall.

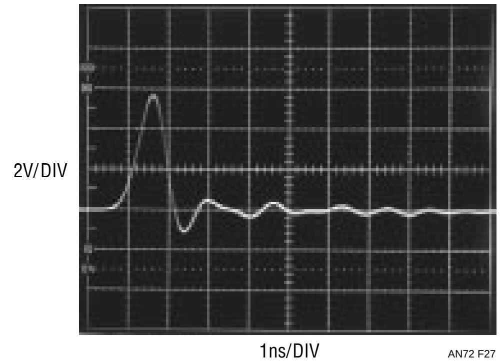



**Figure 27. Test Pulse on the Same 350MHz Oscilloscope Using a 3GHz 10× Probe. Deliberate Poor Grounding Maintains Rippling Residue**

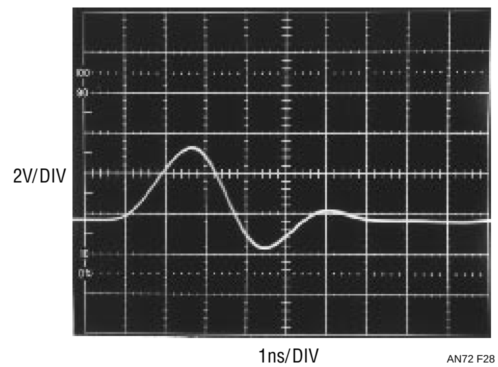



**Figure 28. Test Pulse Measures Only 3V High on a 250MHz ‘Scope with Significant Waveform Distortion. 290MHz 10× Probe Used**

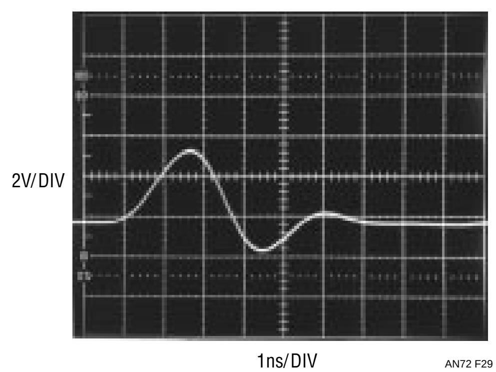



**Figure 29. Test Pulse Measures Under 2V High Using 250MHz ‘Scope and a 100MHz Probe**

In Figure 29, a 100MHz 10× probe (Hewlett-Packard Model 10040A) has been substituted for the 290MHz unit. The oscilloscope and its setup remain the same. Amplitude shrinks below 2V, with commensurate rise and fall times. Cleaned-up grounding eliminates aberrations.

A Tektronix 454A (150MHz) produced Figure 30's trace. The pulse generator was directly connected to the input. Displayed amplitude is about 2V, with appropriate 2ns edges. Finally, a 50MHz instrument (Tektronix 556 with 1A4 plug-in) just barely grunts in response to the pulse (Figure 31). Indicated amplitude is 0.5V, with edges reading about 7ns. That's a long way from the 10V and 350ps that's really there!

A final oscilloscope characteristic is overload performance. It is often desirable to view a small amplitude portion of a large waveform. In many cases the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overload before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overload varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100× overload at 0.005V/division may be very different than at 0.1V/division. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overload must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity which eliminates all off-screen activity. Figure 32 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure 33) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure 34, gain has been further increased and all the features of Figure 33 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see.

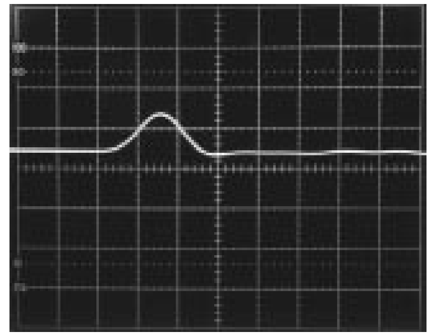



**Figure 30. 150MHz Oscilloscope ($t_{RISE}$ = 2.4ns) with Direct Connection Responds to the Test Pulse**

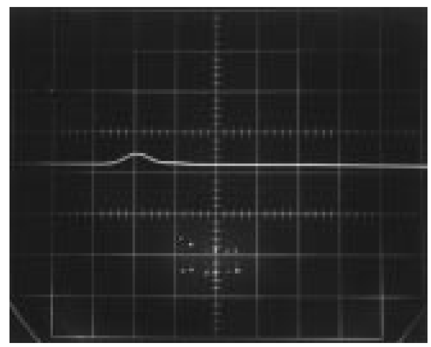



**Figure 31. A 50MHz Instrument Barely Grunts. 10V, 350ps Test Pulse Measures Only 0.5V High with 7ns Rise and Fall Times!**

No new waveform characteristics are observed. Figure 35 brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure 34. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure 36 the gain remains the same, but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point, which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure 37). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

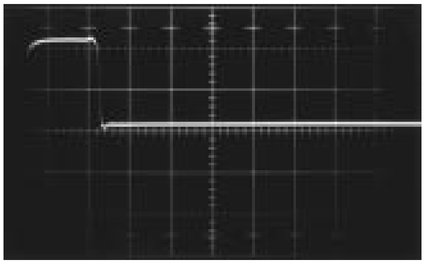



**Figure 32**

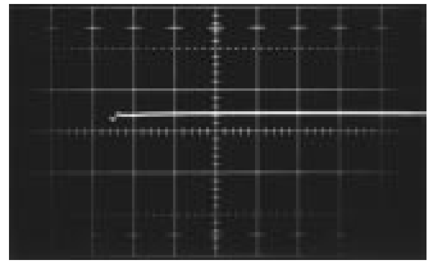



**Figure 33**

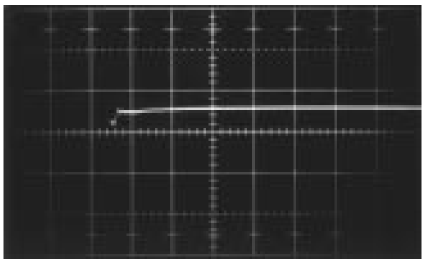



**Figure 34**

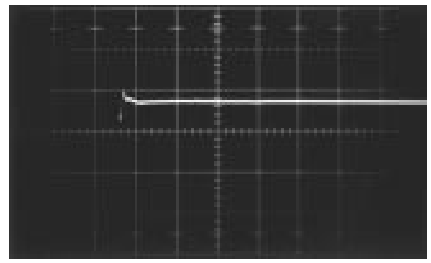



**Figure 35**

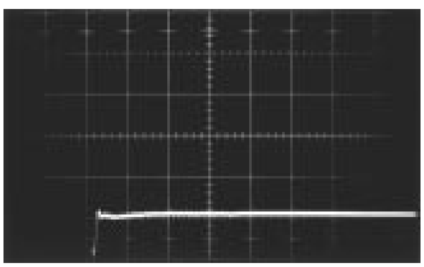



**Figure 36**

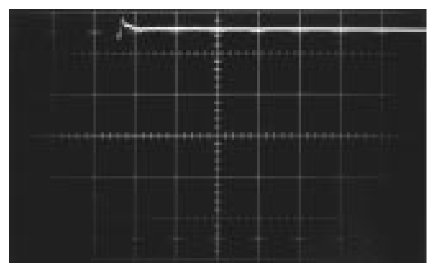



**Figure 37**

**Figures 32 to 37: The Overdrive Limit Is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations**

Differential plug-ins can address some of the issues associated with excessive overdrive, although they cannot solve all problems. Two differential plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7, 1A7A and 7A22 feature 10µV sensitivity, although bandwidth is limited to 1MHz. The units also have selectable highpass and lowpass filters and good high frequency common mode rejection. Tektronix type 1A5, W and 7A13 are differential comparators. They have calibrated DC nulling (slide back) sources, allowing observation of small, slowly moving events on top of common mode DC or fast events riding on a waveform.

A special case is the sampling oscilloscope. By nature of its operation, a sampling 'scope in proper working order is inherently immune to input overload, providing essentially instantaneous recovery between samples. See Reference 8 for additional details.

The best approach to measuring small portions of large waveforms, however, is to eliminate the large signal swing seen by the oscilloscope. Reference 17 discusses applicable techniques in detail.

In summary, although the oscilloscope provides remarkable capability, its limitations must be well understood when interpreting results.[9]

**Note 9:** Additional discourse on oscilloscopes will be found in References 1 and 7 through 10.

### About Ground Planes

Many times in high frequency circuit layout, the term "ground plane" is used, most often as a mystical and ill-defined cure to spurious circuit operation. In fact, there is little mystery to the usefulness and operation of ground planes, and like many phenomena, their fundamental operating principle is surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a wire carrying current (Figure 38) surrounded by radii of magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the wire's current. To compute the wire's inductance requires integrating the field over the wire's length and the total radial area of the field. This implies integrating on the radius from $R = R_W$ to infinity, a very large number. However, consider the case where we have two wires in space carrying the same current in either direction (Figure 39). The fields produced cancel.

In this case, the inductance is much smaller than in the simple wire case and can be made arbitrarily smaller by reducing the distance between the two wires. This reduction of inductance between current carrying conductors is the underlying reason for ground planes. In a normal circuit, the current path from the signal source through its conductor and back to ground includes a large loop area. This produces a large inductance for this conductor which can cause ringing due to LRC effects. It is worth noting that 10nH at 100MHz has an impedance of 6Ω. At 10mA a 60mV drop results.

A ground plane provides a return path directly under the signal carrying conductor through which return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents will always flow through the return path of lowest impedance. In a properly designed ground plane, this path is directly under the signal conductor. In a practical circuit, it is desirable to use one whole side of the PC card (usually the component side for wave solder considerations) as a ground plane and run the signal conductors on the other side. This will give a low inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to AC skin effect (AC currents travel along a conductor's surface). Additionally, they aid the circuit's high frequency stability by referring stray capacitances to ground.

Some practical hints for ground planes are:

1. Utilize a ground plane over as much area as possible on the component side of the board, especially under traces that operate at high frequency.
2. Mount components that conduct substantial fast rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
3. Where common ground potential is important (i.e., at comparator inputs), try to single point the critical components into the ground plane to avoid voltage drops.
4. Keep trace length short. Inductance varies directly with length and no ground plane will achieve perfect cancellation.

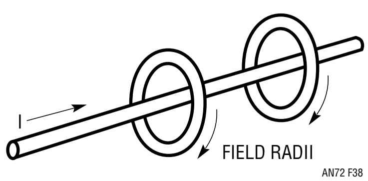



**Figure 38. Single Wire Case**

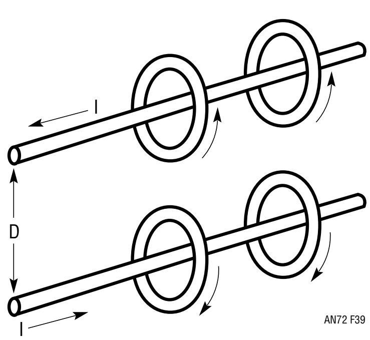



**Figure 39. Two Wire Case**

## About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation were used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure 40. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values so they can absorb long transients, necessitating electrolytic types which have large series R and L.

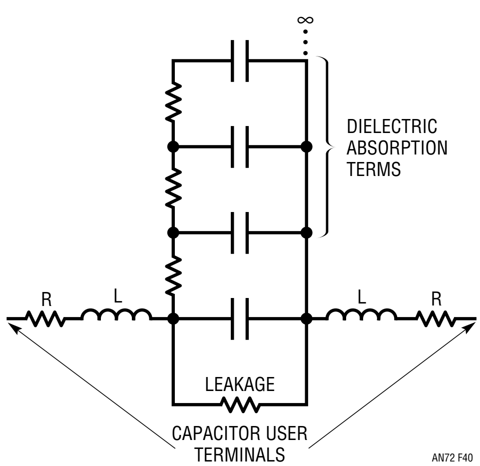



**Figure 40. Parasitic Terms of a Capacitor**

Different types of electrolytics and electrolytic-nonpolar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure 41) and accompanying photos are useful. The photos show the response of five bypassing methods to the transient generated by the test circuit. Figure 42 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure 43 uses an aluminum 10µF electrolytic to considerably cut the disturbance, but there is still plenty of potential trouble. A tantalum 10µF unit offers cleaner response in Figure 44 and the 10µF aluminum combined with a 0.01µF ceramic type is even better in Figure 45. Combining electrolytics with nonpolarized capacitors is a popular way to get good

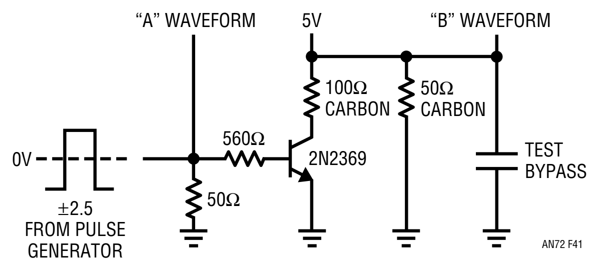



**Figure 41. Bypass Capacitor Test Circuit**

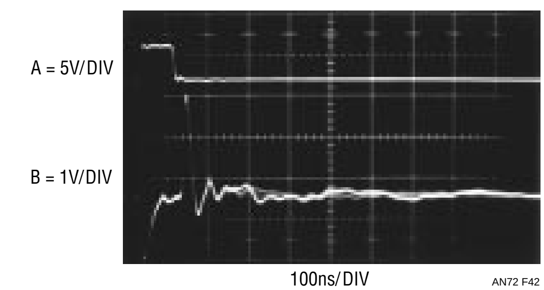



**Figure 42. Response of Unbypassed Line**

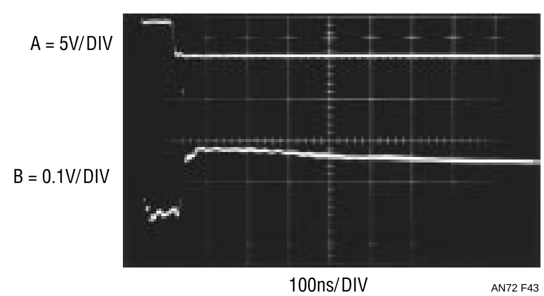



**Figure 43. Response of 10µF Aluminum Capacitor**

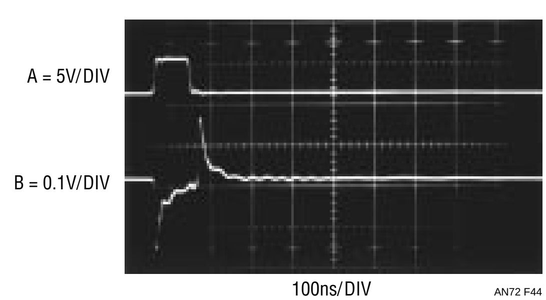



**Figure 44. Response of 10µF Tantalum Capacitor**

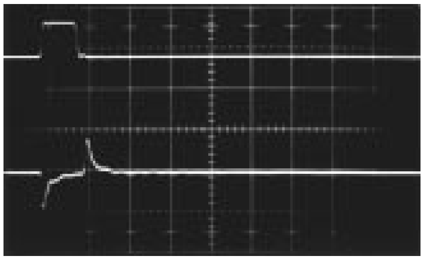



**Figure 45. Response of 10μF Aluminum Paralleled by 0.01μF Ceramic**

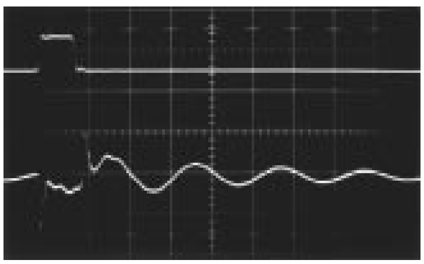



**Figure 46. Some Paralleled Combinations Can Ring. Try Before Specifying!**

response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in Figure 46. Caveat!

**Breadboarding Techniques**

The breadboard is both the designer's playground and proving ground. It is there that Reality resides, and paper (or computer) designs meet their ruler. More than anything else, breadboarding is an iterative procedure, an odd amalgam of experience guiding an innocent, ignorant, explorative spirit. A key is to be willing to try things out, sometimes for not very good reasons. Invent problems and solutions, guess carefully and wildly, throw rocks and see what comes loose. Invent and design experiments, and follow them wherever they lead. Reticence to try things is probably the number one cause of breadboards that "don't work."[10] Implementing the above approach to life begins with the physical construction methods used to build the breadboard.

A high speed breadboard must start with a ground plane. Additionally, bypassing, component layout and connections should be consistent with high speed operations. Because of these considerations there is a common misconception that breadboarding high speed circuits is time consuming and difficult. This is simply not true. For high speed circuits of moderate complexity a complete and electrically correct breadboard can be assembled in 10 minutes if all necessary components are on hand. The key to rapid breadboarding is to identify critical circuit nodes and design the layout to suit them. This permits most of the breadboard's construction to be fairly sloppy, saving time and effort. Additionally, use all degrees of freedom in making connections and mounting components. Don't be bashful about bending IC pins to suit desired low capacitance connections, or air wiring components to achieve rapid or electrically optimum layout. Save time by using components, such as bypass capacitors, as mechanical supports for other components, such as amplifiers. It is true that eventual printed circuit construction is required, but when initially breadboarding forget about PC and production constraints. Later, when the circuit works, and is well understood, PC adaptations can be taken care of.[11]

Once the breadboard seems to work, it's useful to begin thinking about PC layout and component choice for production. Experiment with the existing layout to determine just how sensitive nominally critical points are. Add controlled parasitic terms (e.g., resistors, capacitors and physical layout changes) to test for sensitivity. Gentle touching of suspect points with a finger can yield preliminary indication of sensitivity, giving clues that can be quite valuable.

In conclusion, when breadboarding, design the breadboard to be quick and easy to build, work with and modify. Observe the circuit and listen to what it is telling you before trying to get it to some desired state. Finally, don't hesitate to try just about anything; that's what the breadboard is for. Almost anything you do will cause some result—whether it's good or bad is almost irrelevant. Anything you do that enhances your ability to correlate events occurring on the breadboard can only be beneficial.

**Note 10:** A much more eloquently stated version of this approach is found in Reference 12.
**Note 11:** See Reference 17 for a pictorially enhanced version of this discussion.

This completes the tutorial section. Hopefully, several notions have been imparted. First, in any measurement situation, test equipment characteristics are an integral part of the circuit. At high speed and high precision this is particularly the case. As such, it is imperative to know your equipment and how it works. There is no substitute for intimate familiarity with your tool's capabilities and limitations.[12]

In general, use equipment you trust and measurement techniques you understand. Keep asking questions and don't be satisfied until everything you see on the oscilloscope is accounted for and makes sense.

The LT1394, combined with the precautionary notes listed above, permits fast linear circuit functions that are difficult or impractical using other approaches. Some of the applications presented in the following section represent the state-of-the-art for a particular circuit function. Others show simplified and/or improved ways to implement standard functions by utilizing the comparator's easily accessed speed. All have been carefully (and painfully) worked out and should serve as good idea sources for potential users of the device. Have fun. I did.

## APPLICATIONS

### Crystal Oscillators

Figure 47's circuits are crystal oscillators. In the circuit (a) the resistors at the LT1394's positive input set a DC bias point. The 2k-0.068μF path sets up phase shifted feedback and the circuit looks like a wideband unity-gain follower at DC. The crystal's path provides resonant positive feedback and stable oscillation occurs. The circuit (b) is similar, but supports oscillation frequencies to 30MHz. Above 10MHz, AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, ensuring proper operation.

### Switchable Output Crystal Oscillator

Figure 48 permits crystals to be electronically switched by logic commands. This circuit is similar to the previous examples, except that oscillation is only possible when one of the logic inputs is biased high.

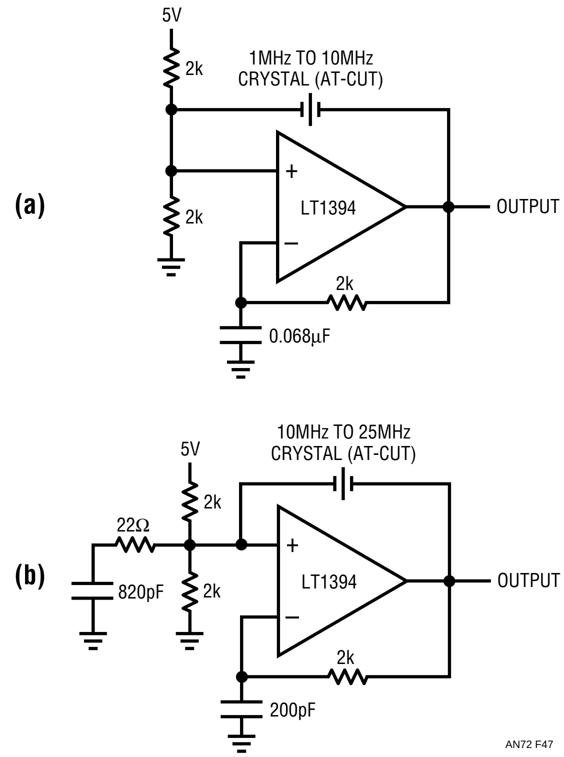



**Figure 47. Crystal Oscillators for Outputs to 30MHz. Circuit (b)'s Damper Network Supresses Overtone Crystal's Harmonic Modes**

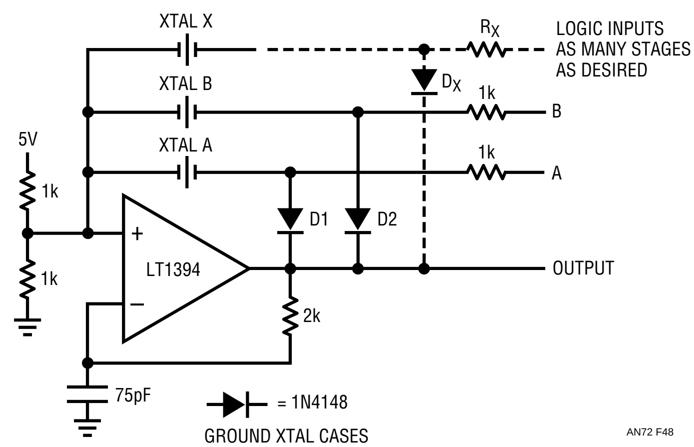



**Figure 48. Switchable Output Crystal Oscillator. Biasing A or B High Places Associated Crystal in Feedback Path. Additional Crystal Branches Are Permissible**

**Note 12:** Further exposition and *kvetching* on this point is given in Reference 13.

### Temperature-Compensated Crystal Oscillator (TXCO)

Figure 49 is a temperature-compensated crystal oscillator (TXCO). This circuit reduces oscillator temperature drift by inserting a temperature-dependent compensatory correction into the crystal's frequency trimming network. This open-loop correction technique relies on matching the oscillator's frequency versus temperature characteristic, which is quite repeatable.

The LT1394 and associated components form the crystal oscillator, operating similarly to Figure 47's examples. The LM134, a temperature-dependent current source, biases A1. A1 takes gain referred to the LM134's output and the negative offset supplied via the 470kΩ-LT1004 reference path. Note that the LT1004's negative voltage bias is bootstrapped from the oscillator's output, maintaining single supply operation. This arrangement delivers temperature-dependent bias to the varactor diode, causing a scaled variation in the crystal's resonance versus ambient temperature. The varactor's bias-dependent capacitance shift pulls crystal frequency to complement the circuit's temperature drift. The simple first order fit provided by the compensation is very effective. Figure 50 shows results.

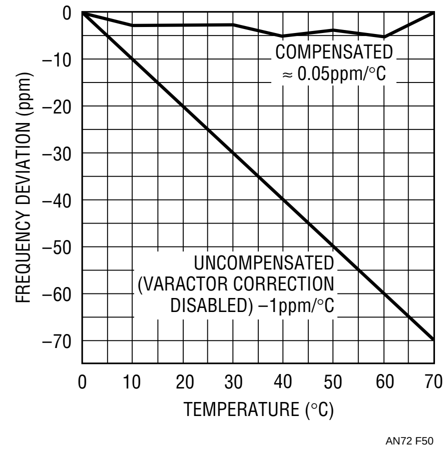



**Figure 50. Figure 49's Compensated vs Uncompensated Temperature Dependence. First Order Compensation Reduces Oscillator Drift to 0.05ppm/°C**

The –70ppm frequency shift over 0°C to 70°C is corrected within a few ppm. The "FREQ SET" trim also biases the varactor, allowing accurate output frequency setting. It is worth noting that better compensation is possible by including higher order terms in the temperature-to-voltage conversion.

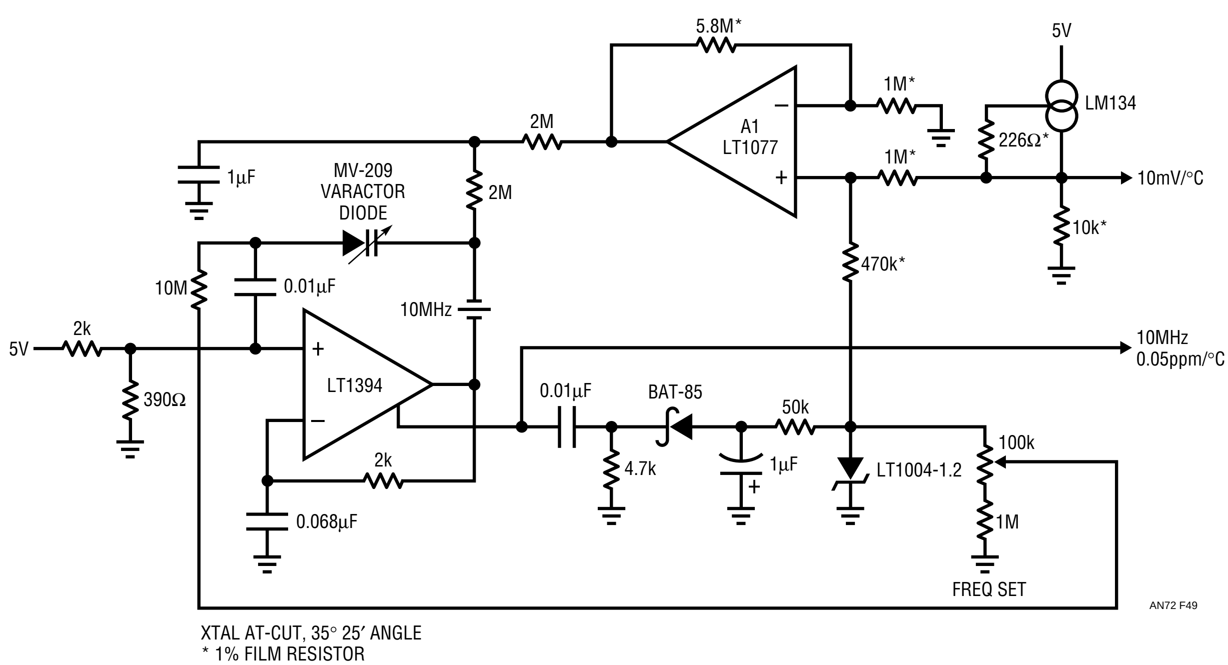



**Figure 49. Temperature-Compensated 10MHz Crystal Oscillator. Temperature-Dependent Varactor Bias Reduces Drift by 20:1**

### Voltage-Controlled Crystal Oscillator (VCXO)

Figure 51, also a variant of the basic crystal oscillator, permits voltage tuning the output frequency. Such voltage-controlled crystal oscillators (VCXO) are often employed where slight variation of a stable carrier is required. This example is specifically intended to provide a 4× NTSC sub-carrier tunable oscillator suitable for phase locking.

The LT1394 is set up as a crystal oscillator, operating similarly to Figure 47(a). The varactor diode is biased from the tuning input. The tuning network is arranged so a 0V to 5V drive provides a reasonably symmetric, broad tuning range around the 14.31818MHz center frequency. The indicated selected capacitor sets tuning bandwidth. It should be picked to complement loop response in phase locking applications. Figure 52 is a plot of tuning input voltage versus frequency deviation. Tuning deviation from the 4× NTSC 14.31818MHz center frequency exceeds ±240ppm for a 0V to 5V input.

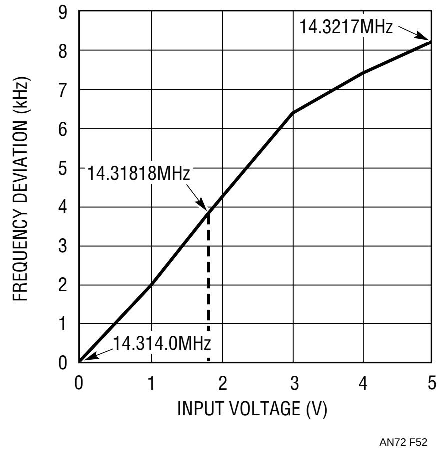



**Figure 52. Control Voltage vs Output Frequency for Figure 51. Tuning Deviation from Center Frequency Exceeds ±240ppm**

### Voltage-Tunable Clock Skew Generator

It is sometimes necessary to generate pairs of identical clock signals that are phase skewed in time. Further, it is desirable to be able to set the amount of time skew via a tuning voltage. Figure 53's circuit does this by utilizing comparators to digitize phase information from a varactor-tuned time domain bridge. A 0V to 2V control signal provides ≈ ±10ns of output skew. The input is applied to the CMOS inverters, which deliver noninverting drive to the bridge network (Trace A, Figure 54). The bridge, essentially composed of two RC sections, responds in ramp fashion at both of its outputs (Trace B is "fixed" output, Trace C is "skewed"output). The "skewed" bridge half's capacitance is tuned by a varactor diode, biased

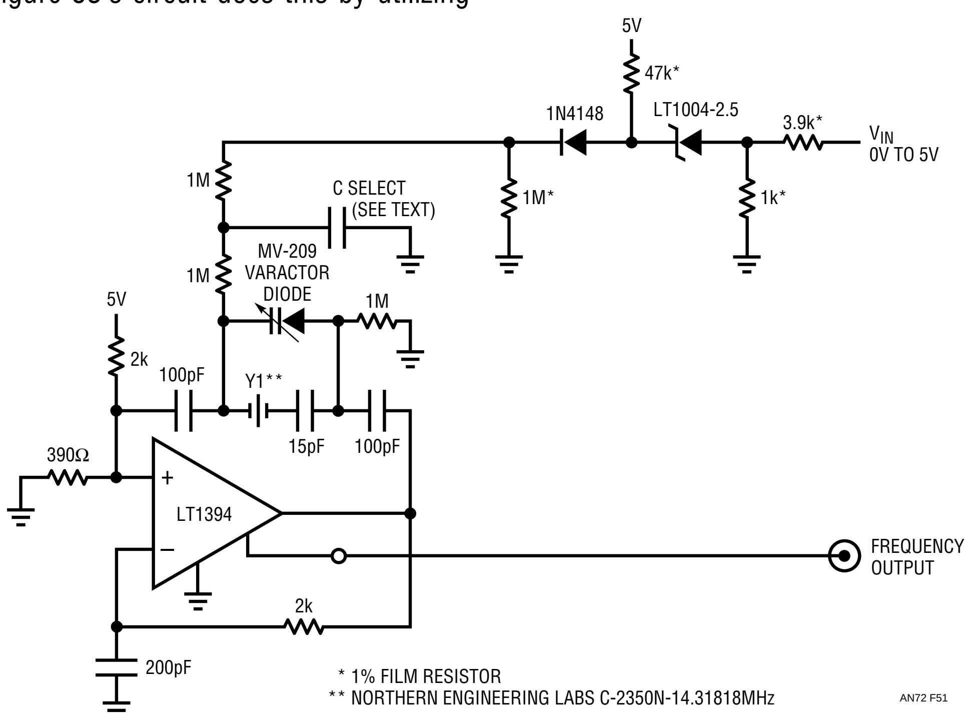



**Figure 51. A 4× NTSC Sub-Carrier Voltage-Tunable Crystal Oscillator. Tuning Range and Bandwidth Accommodate Variety of Phase Locked Loops**

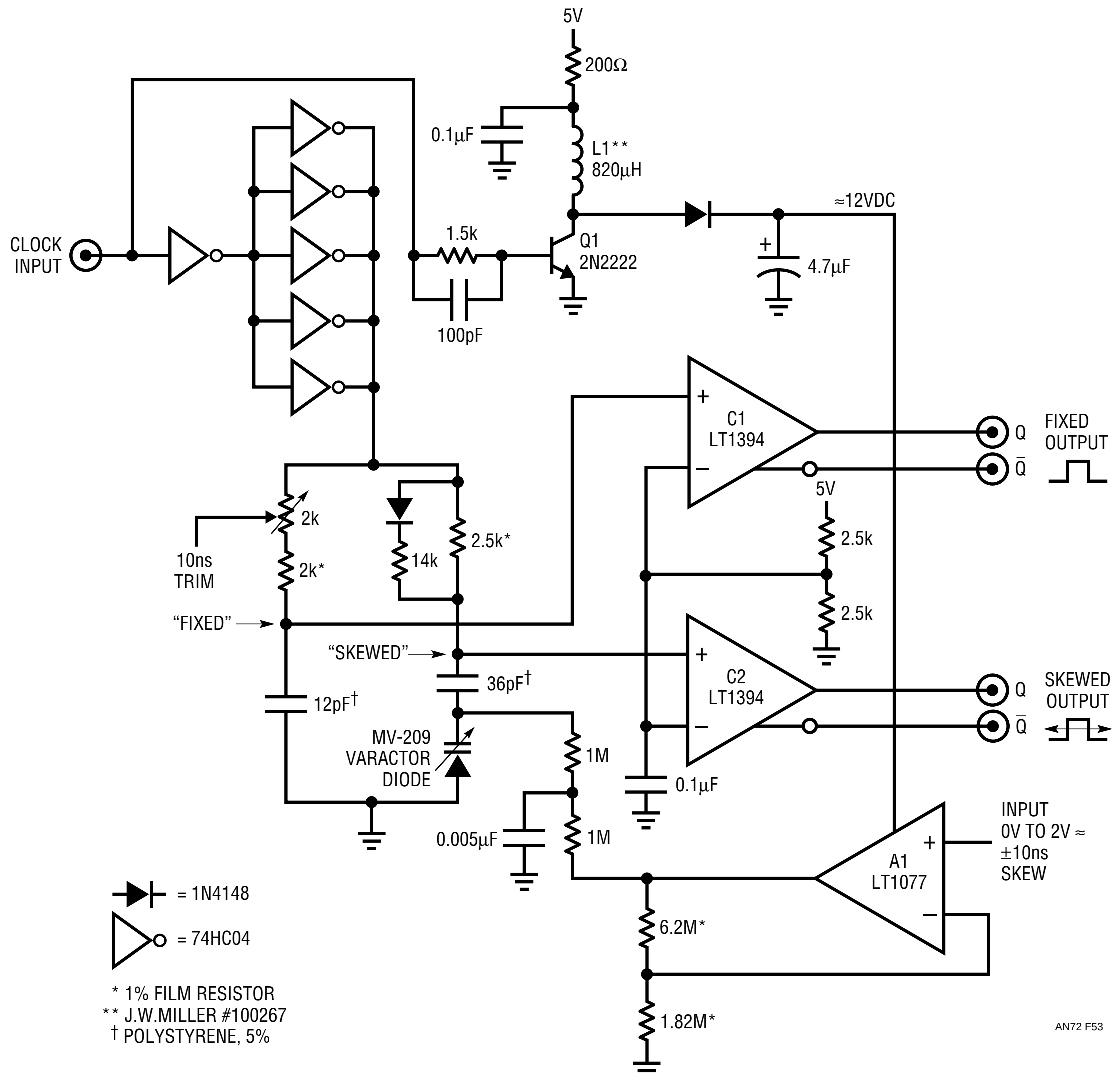



**Figure 53. Comparators Extract Phase Difference from Varactor- Tuned Bridge, Permitting Controllable Clock Skew**

from A1, and hence the control input. The comparators, referenced to 1/2 supply voltage, trigger (Traces D and E are C1 and C2 output, respectively) when their positive inputs exceed the reference point. The time skew of this response is determined by imbalance in the bridge's RC time constants, which is controlled via the voltage input. The diode-resistor network across the 2.5k bridge resistor compensates for ramp-induced variation of varactor capacitance, enhancing control symmetry. Q1 and associated components form a simple voltage boost stage, enabling A1 to supply adequate varactor bias. The bridge's ratiometric operation permits almost 100:1 power supply rejection ratio over a $4.5V_{IN}$ to $5.5V_{IN}$ range. To trim this circuit, put in 2V and adjust the 2k potentiometer for 10ns

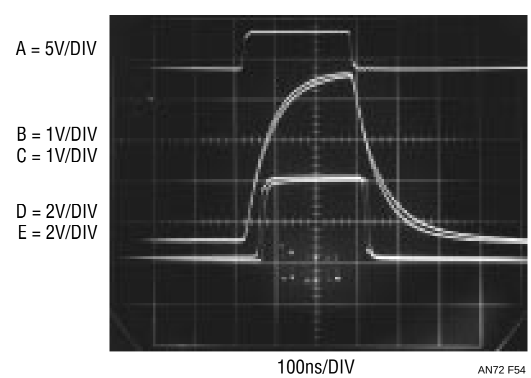



**Figure 54. Clocked (Trace A), Varactor-Tuned Bridge Has Phase Shifted Outputs (Traces B and C). Comparators (Traces D and E) Digitize Information, Providing Output**

skew in the outputs. Over a 0V to 2V range, output skew will continuously vary from –10ns through 0, to 10ns.

### Simple 10MHz Voltage-to-Frequency Converter

Figure 55 is a voltage-to-frequency converter. A 0V to 2.5V input produces a 0Hz to 10MHz output with 40dB of dynamic range, 1% linearity and 400ppm/°C gain drift. Power supply rejection is 0.5% for 4.75V to 5.25V supply excursions.

To understand circuit operation, assume C1's positive input is slightly below its negative input. The input voltage causes a positive-going ramp at C1's positive input (Trace A, Figure 56). C1's output is low, biasing the CMOS inverters high. This allows current flow from diode Q1's collector, through the CMOS inverter supply pin to the 10pF capacitor. The 4.7µF capacitor provides high frequency bypass, maintaining low impedance at Q1's collector. Diode connected Q3 provides a path to ground. The voltage the 10pF capacitor charges to is a function of Q1's collector potential and Q3's drop. When the ramp at C1's positive input goes high enough, C1's output goes high and the paralleled inverters switch low (Trace B). This action pulls current from C1's positive input capacitor via the Q4-10pF route (Trace D). This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output low and the paralleled inverters high. The 8pF capacitor at C1's inverting output furnishes AC positive feedback to C1's negative input (Trace C). This ensures that C1's output remains high long enough for a complete discharge of the 10pF unit. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 8pF capacitor's feedback decays, C1 again switches high and the entire cycle repeats. The oscillation frequency depends directly on the input-derived current.

The LT1004 is the circuit's voltage reference, with Q1 and Q2 temperature compensating Q3 and Q4.

Start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high, causing the paralleled inverters to go low. After a time determined by the 1M-1000pF RC the associated lone inverter goes high. This lifts C1's negative input and grounds the positive input with Q5, initiating normal circuit action.

To calibrate this circuit, apply 2.5V and adjust the 10k potentiometer for a 10MHz output.

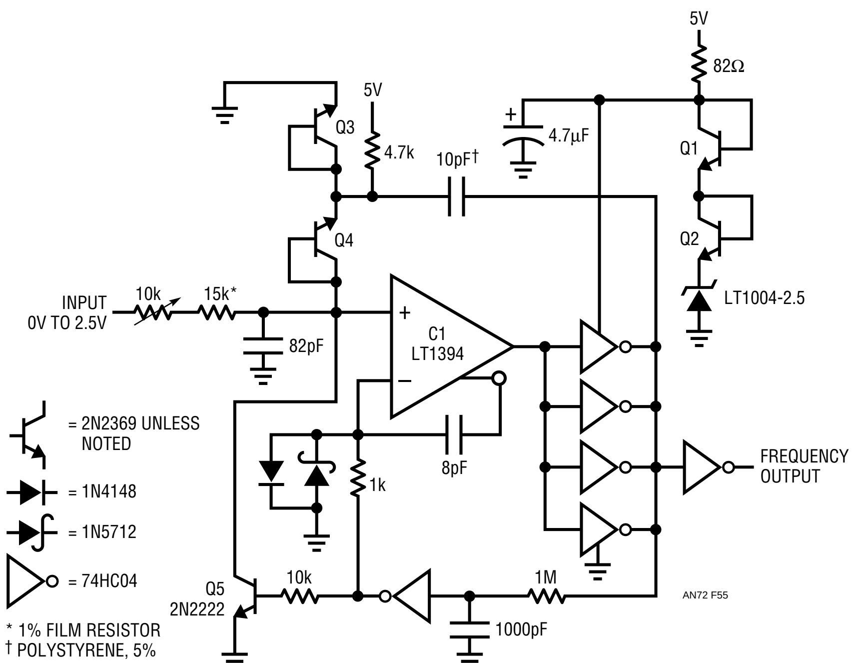



**Figure 55. Simple Charge Pump-Based 10MHz Voltage-to-Frequency Converter Has 40dB Dynamic Range, Operates from 5V Supply**

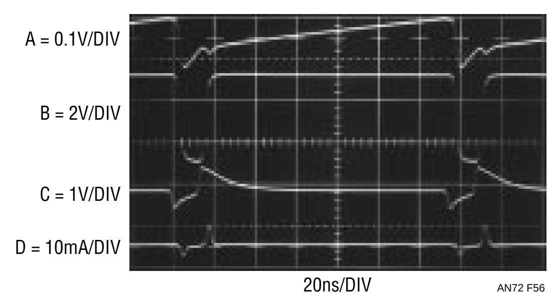



**Figure 56. Waveforms for the 10MHz Voltage-to-Frequency Converter. Charge Pump-Based Feedback Provides Linearity and Fast Response to Input**

### Precision 1Hz to 10MHz Voltage-to-Frequency Converter

Significant performance improvements over the previous circuit are achievable if increased complexity is tolerable. The LT1394 and the LT1122 high speed FET amplifier combine to form a high speed V/F converter in Figure 57. A variety of circuit techniques are used to achieve a 1Hz to 10MHz output. Overrange to 12MHz ($V_{IN}$ = 12V) is provided. This circuit has a wider dynamic range (140dB or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is ten times faster than currently available monolithic V/Fs. The theory of operation is based on the identity Q = CV.

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency that permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

0.05µV/°C offset drift performance is obtained by stabilizing A1 with A2, a chopper-stabilized op amp. A2 measures the DC value of the negative input, compares it to ground, and forces the positive input to maintain offset balance in A1. Note that A2 is configured as an integrator and cannot see high frequency signals. It functions only at DC and low frequency.

A1 is arranged as an integrator with a 68pF feedback capacitor. When a positive voltage is applied to the input, A1's output integrates in a negative direction (Trace A, Figure 58). During this period, C1's inverting output is low. The paralleled HCMOS inverters form a reference voltage switch. The reference voltage is established by the LM134 current source driven LT1034's and the Q3-Q4 combination. Additionally, a small input voltage-related term is summed into the reference, improving overall circuit linearity. A3-A4 provides low drift buffering, presenting a

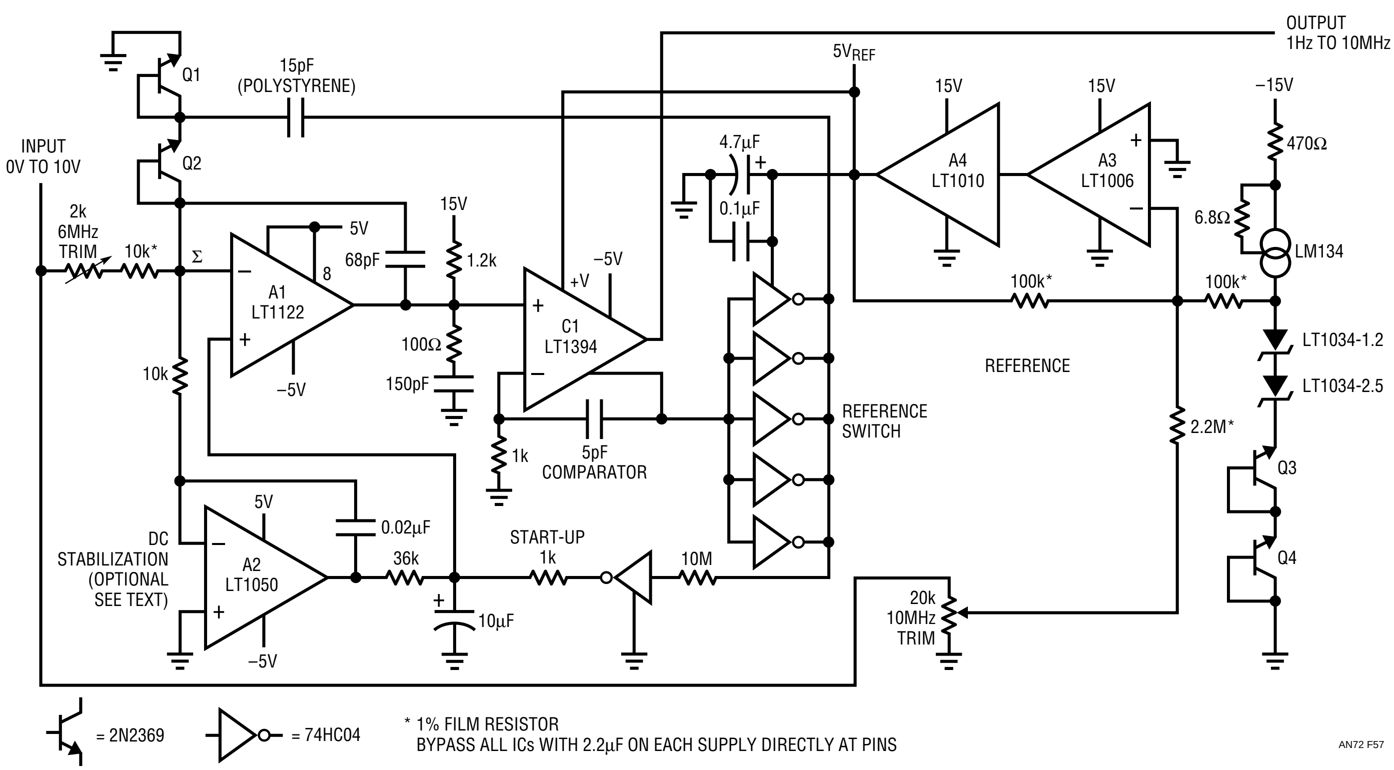



**Figure 57. A Very High Performance 1Hz to 10MHz Voltage-to-Frequency Converter. Linearity is 0.03% with 50ppm/°C Drift**

low impedance reference to the paralleled inverter's supply pin. The HCMOS outputs give low resistance, essentially errorless switching. The reference switch's output charges the 15pF capacitor via Q1's path.

When A1's output crosses zero, C1's inverting output goes high and the reference switch (Trace B) goes to ground. This causes the 15pF unit to dispense charge into the summing node via Q2's $V_{BE}$. The amount of charge dispensed is a direct function of the voltage the 15pF unit was charged to (Q = CV). Q1 and Q2 are temperature compensated by Q3 and Q4 in the reference string. The current through the 15pF unit (Trace C) reflects the charge pumping action. The removal of current from A1's summing junction (Trace D) causes the junction to be driven very quickly negative. The initial negative-going 15ns transient at A1's output is due to amplifier delay. The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (Trace A) slew limits as it attempts to regain control of the summing node. The class A 1.2kΩ pull-up and the RC damper at A1's output minimize erroneous output movement, enhancing this slew recovery. The amount of time the reference switch remains at ground depends on how long it takes A1 to recover and the 5pF-1000Ω time constant at C1. This 60ns interval is long enough for the 15pF unit to fully discharge. After this, C1 changes state, the reference switch swings positive, the capacitor is recharged and the entire cycle repeats. The frequency at which this oscillation occurs is directly related to the voltage input-derived current into the summing junction. Any input current will require a corresponding oscillation frequency to hold the summing point at an average value of 0V.

Maintaining this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to achieving 10MHz full-scale operating frequency is the ability to transmit information around the loop as quickly as possible. The discharge-reset sequence is particularly critical and is detailed in Figure 59. Trace A is the A1 integrator output. Its ramp output crosses 0V at the first left vertical graticule division. A few nanoseconds later, C1's inverting output begins to rise (Trace B), switching the reference switch to ground (Trace C). The reference switch begins to head towards ground about 16ns after A1's output crosses 0V. 2ns later, the summing point (Trace D) begins to go negative as current is pulled from it through the 15pF capacitor. At 25ns, C1's inverting output is fully up, the reference switch is at ground, and the summing point has been pulled to its negative extreme. Now, A1 begins to take control. Its output (Trace A) slews rapidly in the positive direction, restoring the summing point. At 60ns, A1 is in control of the summing node and the integration ramp begins again.

Start-up and overdrive conditions could force A1's output to go to the negative rail and stay there. The AC-coupled nature of the charge dispensing loop can preclude normal operation and the circuit may latch. The remaining HCMOS inverter provides a watchdog function for this condition. If A1's output remains negative the reference switch tries to stay at ground. The remaining inverter goes high, lifting A1's positive input. This causes A1's output to slew positive, initiating normal circuit action. The 1k-10µF combination and the 10M-inverter input capacitance limit start-up loop bandwidth, preventing unwanted outputs.

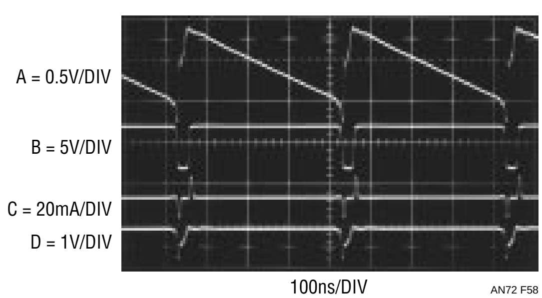



**Figure 58. Precision 10MHz Voltage-to-Frequency's Operating Waveforms. LT1122 Integrator Is Completely Reset in 60ns**

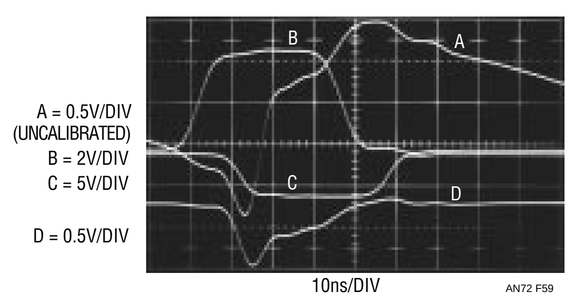



**Figure 59. Detail of 60ns Reset Sequence (Whoosh!)**

The LM134 current source driving the reference string has a built in 0.33%/°C thermal coefficient, causing slight voltage modulation in the Q3-Q4 pair over temperature. This small change (≈120ppm/°C) opposes the –120ppm/°C drift in the 15pF polystyrene capacitor, aiding overall circuit tempco.

To trim this circuit, apply exactly 6V at the input and adjust the 2kΩ potentiometer for 6.000MHz output. Next, put in exactly 10V and trim the 20k unit for 10.000MHz output. Repeat these adjustments until both points are fixed. A2's low drift eliminates a zero adjustment. If operation below 600Hz is not required, A2 and its associated components may be deleted.

Linearity of this circuit is 0.03% with full-scale drift of 50ppm/°C. Zero point error, controlled by A2, is 0.05Hz/°C.

### Fast, High Impedance, Variable Threshold Trigger

A frequent requirement in instrumentation is a fast trigger with a variable threshold. Often, a high impedance input is also required. Figure 60 meets these requirements. Comparator C1 is the basic trigger, with threshold voltage set at its negative input. Source follower Q1 provides high impedance with about 2pF input capacitance and 50pA bias current. Normally, Q1's source bias point would be uncertain and drifty, but stabilization techniques eliminate this concern. A1 measures filtered versions of Q1's gate and source voltages. A1's output biases Q2, forcing Q1's channel current to whatever value is required to equalize A1's inputs, and hence Q1's gate and source voltages. A1's input filtering and roll-off are far slower than input frequencies of interest; its action does not interfere with the circuit's main signal path. The 330pF capacitor prevents fast edges coupled through Q2's collector base junction from influencing A1's operation.

Q1 should contribute negligible timing error to minimize overall delay. Figure 61's photo verifies Q1's wideband operation. Trace B, Q1's source, lags the input (Trace A) by only 300ps. Input, FET buffer output and C1 output appear as Traces A, B and C, respectively in Figure 62. As before, the FET buffer is seen to contribute small timing error, and C1's output is about 8ns delayed from the input.

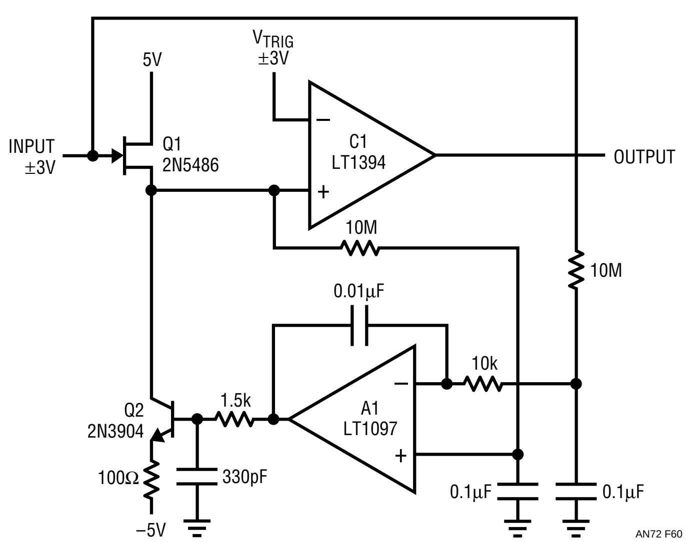



Figure 60. Buffer Provides 2pF, 50pA Input Characteristics for Fast Trigger. Amplifier-Stabilized Biasing Eliminates FET Offset

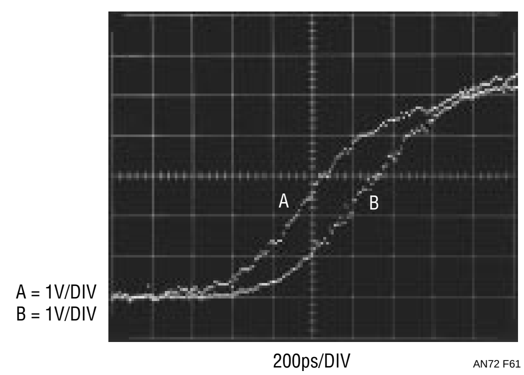



Figure 61. Trigger Buffer's 300ps Delay Minimizes Timing Error. 4GHz Sampling Oscilloscope's Output Is a Series of Dots

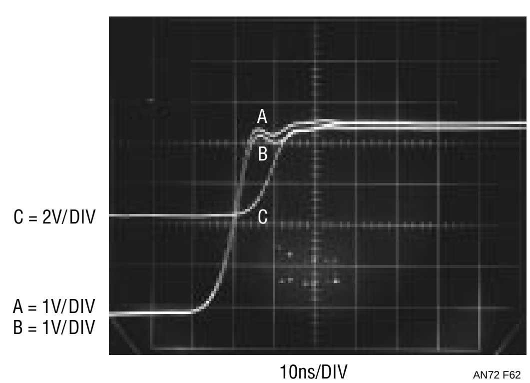



Figure 62. Input (Trace A), FET Source (Trace B) and Output (Trace C) Waveforms for the Trigger. Total Delay Is 8ns

## High Speed Adaptive Trigger Circuit

Line and fibre-optic receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 63 triggers on 2mV to 175mV signals from 100Hz to 45MHz while operating from a single 5V rail. A1, operating at a gain of 15, provides wideband AC gain. The output of this stage biases a 2-way peak detector (Q1 through Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of the midpoint of A1's output signal appears at the junction of the 500pF capacitor and the 3MΩ units. This point always sits midway between the signal's excursions, egardless of absolute amplitude. This signal-adaptive voltage is buffered by A2 to set the trigger voltage at the LT1394's positive input. The LT1394's negative input is biased directly from A1's output. The LT1394's output, the circuit's output, is unaffected by >85:1 signal amplitude variations. Bandwidth limiting in A1 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

Figure 64 shows operating waveforms at 45MHz. Trace A's input produces Trace B's amplified output at A1. The comparator's output is Trace C.

Split supply versions of this circuit can achieve bandwidths to 50MHz with wider input operating range (see Reference 17).

## 18ns, 500μV Sensitivity Comparator

The ultimate limitation on comparator sensitivity is available gain. Unfortunately, increasing gain invariably involves giving up speed. The gain vs. speed trade-off in a fast comparator is usually a practical compromise designed to satisfy most applications. Some situations, however, require more sensitivity (e.g., higher gain) with

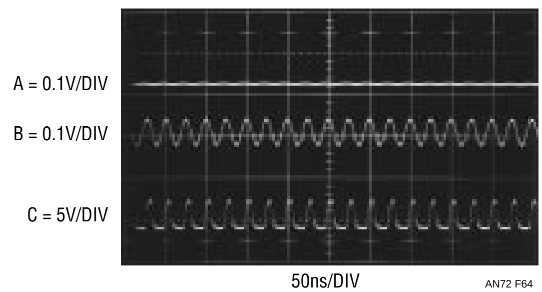



**Figure 64. Adaptive Trigger Responding to a 40MHz, 5mV Input. Input Amplitude Variations from 2mV to 175mV Are Accommodated**

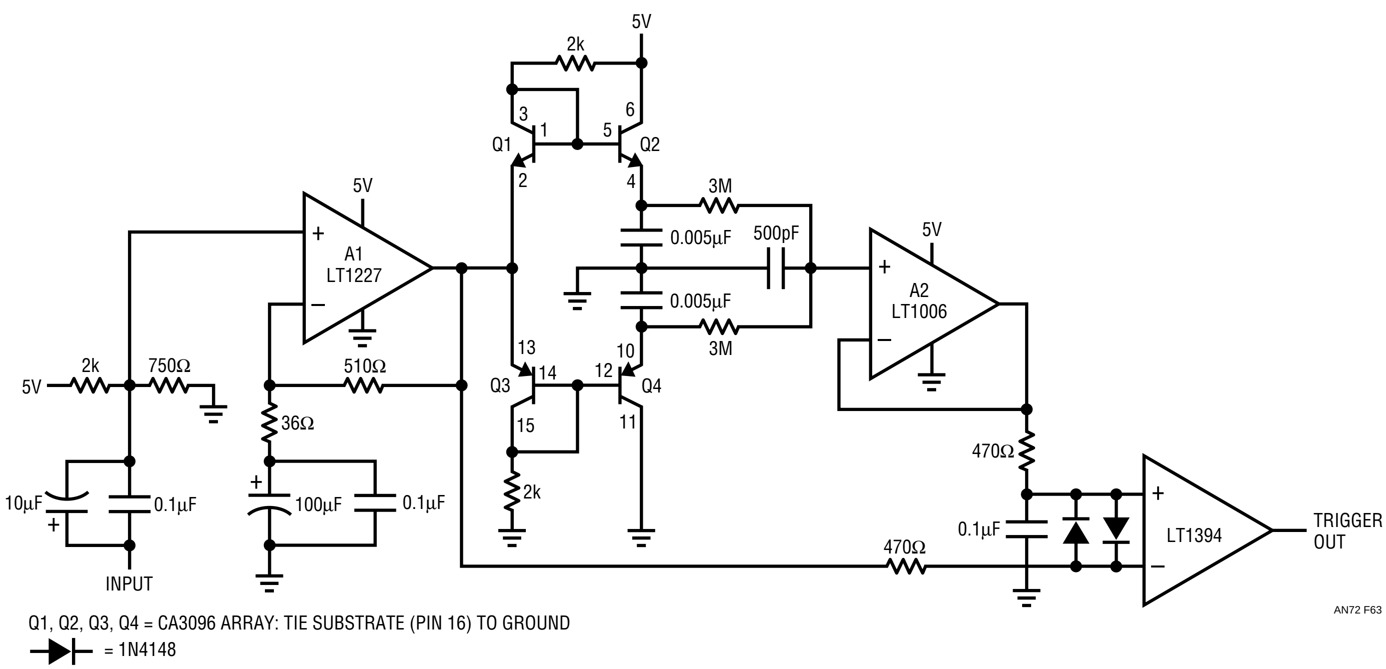



**Figure 63. 45MHz Single Supply Adaptive Trigger. Output Comparator's Threshold Varies Ratiometrically with Input Amplitude, Maintaining Data Integrity over >85:1 Input Amplitude Range**

minimal impact on speed. Figure 65's circuit adds a differential preamplifier ahead of the LT1394, increasing gain. This permits 500μV comparisons in 18ns. A parallel path DC stabilization approach eliminates preamplifier drift as an error source. A1 is the differential preamplifier, operating at a gain of 100. Its output is AC-coupled to the LT1394. A1 has poorly defined DC characteristics, necessitating some form of DC correction. A2 and A3, operating at a differential gain of 100, provide this function. They differentially sense a band limited version of A1's inputs and feed DC and low frequency amplified information to the comparator. The low frequency roll-off of A1's signal path complements A2-A3's high frequency roll-off. The summation of these two signal channels at the LT1394 inputs results in flat response from DC to high frequency.

Figure 66 shows waveforms for the high gain comparator. Trace A is a 500μV overdrive on a 1mV step applied to the circuit's positive input (negative input grounded). Trace B shows the resulting amplified step at A1's positive output. Trace C is A2's band limited output. A1's wideband output combines with A2's DC corrected information to yield the correct, amplified composite signal at the LT1394's positive input in Trace D. The LT1394's output is Trace E. Figure 67 details circuit propagation delay. The output responds in 18ns to a 500μV overdrive on a 1mV step. Figure 68 plots response time versus overdrive. As might be expected, propagation delay decreases at higher overdrives. A1's noise limits usable sensitivity.

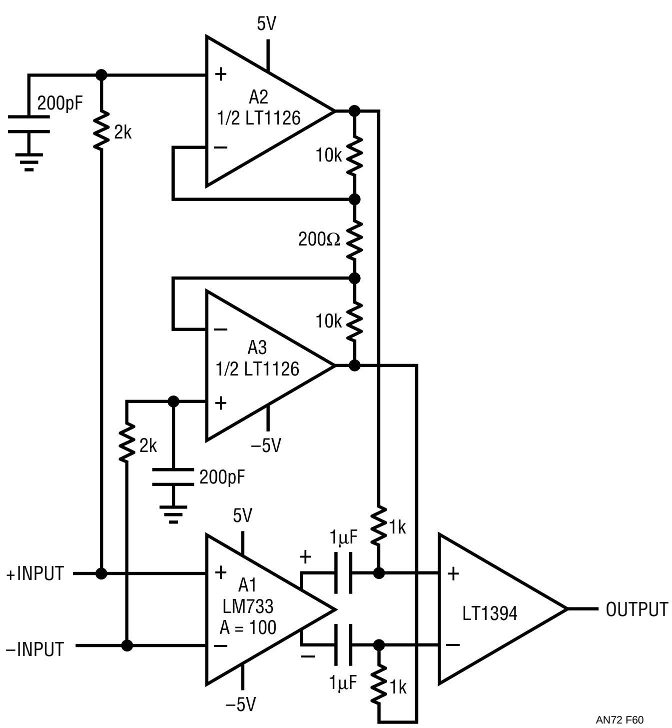



Figure 65. Parallel Preamplified Paths Allow 18ns Comparator Response to 500μV Overdrive

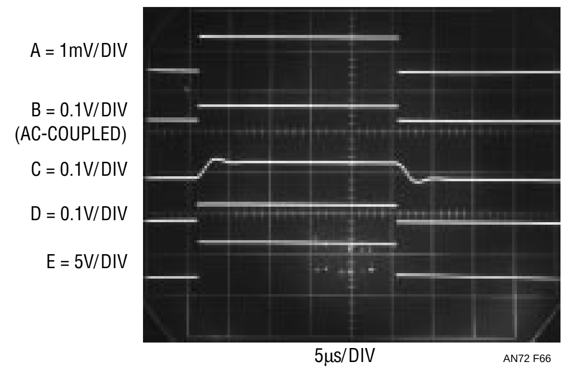



**Figure 66. 500μV Input (Trace A) Is Split into Wideband and Low Frequency Gain Paths (Traces B and C) and Recombined (Trace D). Comparator Output Is Trace E**

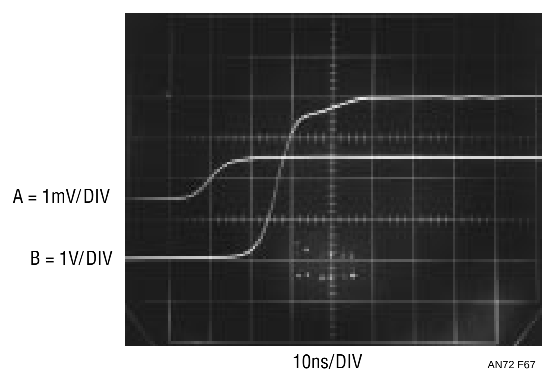



**Figure 67. Parallel Path Comparator Shows 18ns Response (Trace B) to 500μV Overdrive (Trace A)**

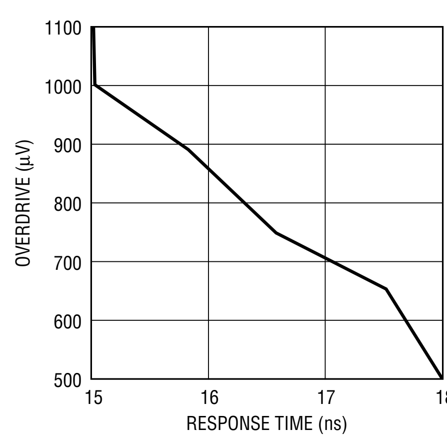



**Figure 68. Response Time vs Overdrive for the Composite Comparator**

### Voltage-Controlled Delay

The ability to set a precise, predictable delay has broad application in pulse circuitry. Figure 69's configuration sets a 0 to 300ns delay from a corresponding 0V to 3V control voltage. It takes advantage of the LT1394's speed and the clean dynamics of an emitter switched current source.

Q1 and Q2 form a current source that charges the 1000pF capacitor. When the trigger input is high (Trace A, Figure 70) both Q3 and Q4 are on. The current source is off and Q2's collector (Trace B) is at ground. The latch input at the LT1394 prevents it from responding and its output remains high. When the trigger input goes low, the LT1394's latch input is disabled and its output drops low. Q4's collector (Trace C) lifts and Q2 comes on, delivering constant current to the 1000pF capacitor (Trace B). The resulting linear ramp at the LT1394's positive input is compared to the delay programming voltage input. When a crossing occurs, the comparator goes high (Trace D). The length of time the comparator was low is directly proportional to the delay programming voltage. The fast switching and ramp linearity permits 1ns accuracy and 100ps repeatability. Figure 71, a high speed expansion of the current source turn-on, details the clean switching. Q4 goes off within 2ns of the trigger input (Trace A) dropping low, enabling the current source (Q2's emitter is Trace C). Concurrently, the 1000pF capacitor's ramp (Trace B) begins. The LT1394's output (Trace D) drops low about 7ns later, returning high after crossing (in this case) a relatively low programming voltage. Figure 72 juxtaposes the waveforms differently, permitting enhanced study of circuit timing. Switching begins with the input trigger falling low (Trace A). The ramp (Trace C) begins 3ns after the current source turns on (Q2 emitter is Trace D). The output pulse (Trace B) begins about 4ns later.

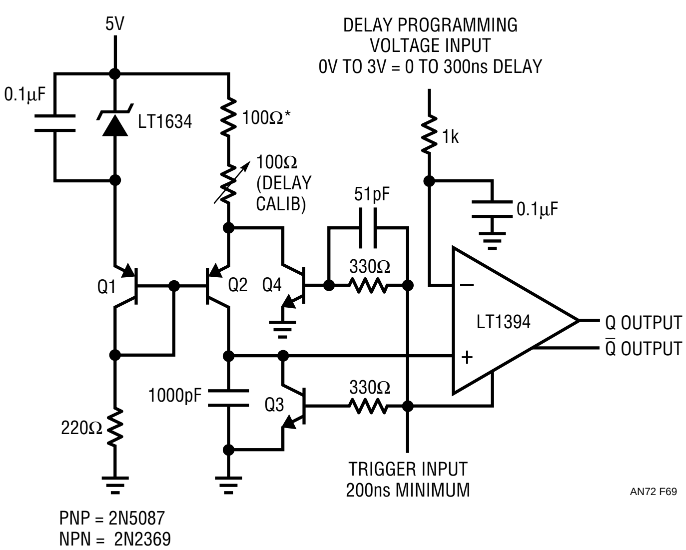



**Figure 69. Fast, Precise, Voltage-Controlled Delay. Emitter Switched Current Source Has Clean, Predictable Dynamics**

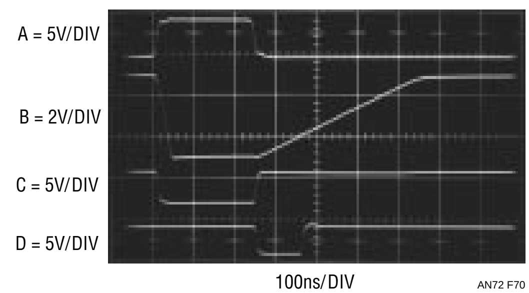



**Figure 70. Voltage-Controlled Delay's Waveforms. Programming Voltage Determines Delay Between Input (Trace A) Falling Edge and Output (Trace D) Rising Edge. High Linearity Timing Ramp (Trace B) Permits 1ns Accuracy and 100ps Repeatability**

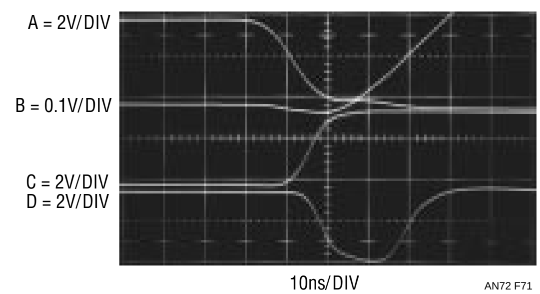



**Figure 71. High Speed Expansion of Figure 70. Ramp (Trace B) Begins When Trigger (Trace A) Falls and Current Source Turns On (Trace C). Trace D is Output**

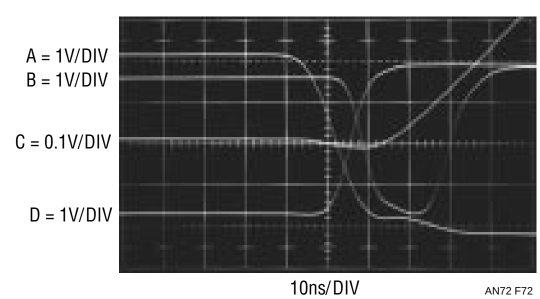



**Figure 72. Delay's Output Switching Begins with Trigger Falling Low (Trace A). Ramp (Trace C) Starts 3ns After Current Source Turn-On (Trace D). Output (Trace B) Begins 4ns Later**

To calibrate this circuit apply a trigger input and 3V to the programming input. Adjust the 100Ω trim for a 300ns width at the LT1394's output.

### 10ns Sample-and-Hold

Figure 73's 10ns sample-and-hold applies the previous circuit. This sample-hold circuit is extremely fast, although it can only be used with repetitive signals. Here, C1 drives differential integrator A1's input. Feedback from the integrator back to C1 closes a loop around the circuit. Figure 74 shows what happens when a waveform (Trace A) is applied to the input. C2 generates a trigger signal for a programmable delay generator identical to the previously described circuit. The 74121 one-shot is triggered from the delay's output. Its Q output produces a 30ns pulse which is fed into a logic network with its $\overline{Q}$ signal. The two inverter delays in Q's path give its associated gate a shorter duration output (Trace C) than $\overline{Q}$'s gate (Trace B). The last gate subtracts these two signals and generates a 10ns spike. This is inverted (Trace D) and fed to C1's latch pin. Each time the latch is enabled the comparator responds to the condition of the summing junction at its "+" input. If summing error is positive, A1 pulls current. If the error is negative, A1 sources current to the junction. After a number of input cycles, A1's output settles at a DC value that is the same as the level sampled during the time the latch is enabled. The delay's voltage programming allows the 10ns sampling "window" to be positioned anywhere on the input waveform.

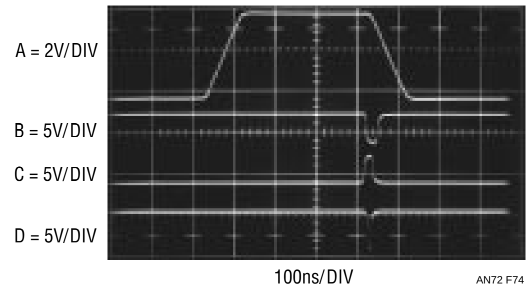



**Figure 74. Sampling Pulse (Trace D) May Be Positioned at Desired Point on Input Waveform (Trace A)**

### Programmable, Sub-Nanosecond Delayed Pulse Generator

The preceding circuit's 10ns wide sampling window limits sampling speed. Faster sampling requires narrower pulses. This circuit uses an avalanche pulse generator[13] to create extremely short duration events. The combination of a controllable, calibrated delay and a very fast pulse generator has broad applicability in fast sampling circuitry.

**Note 13:** See References 17, 20, 22, 27 and 28 for background on avalanche pulse generator theory and practice.

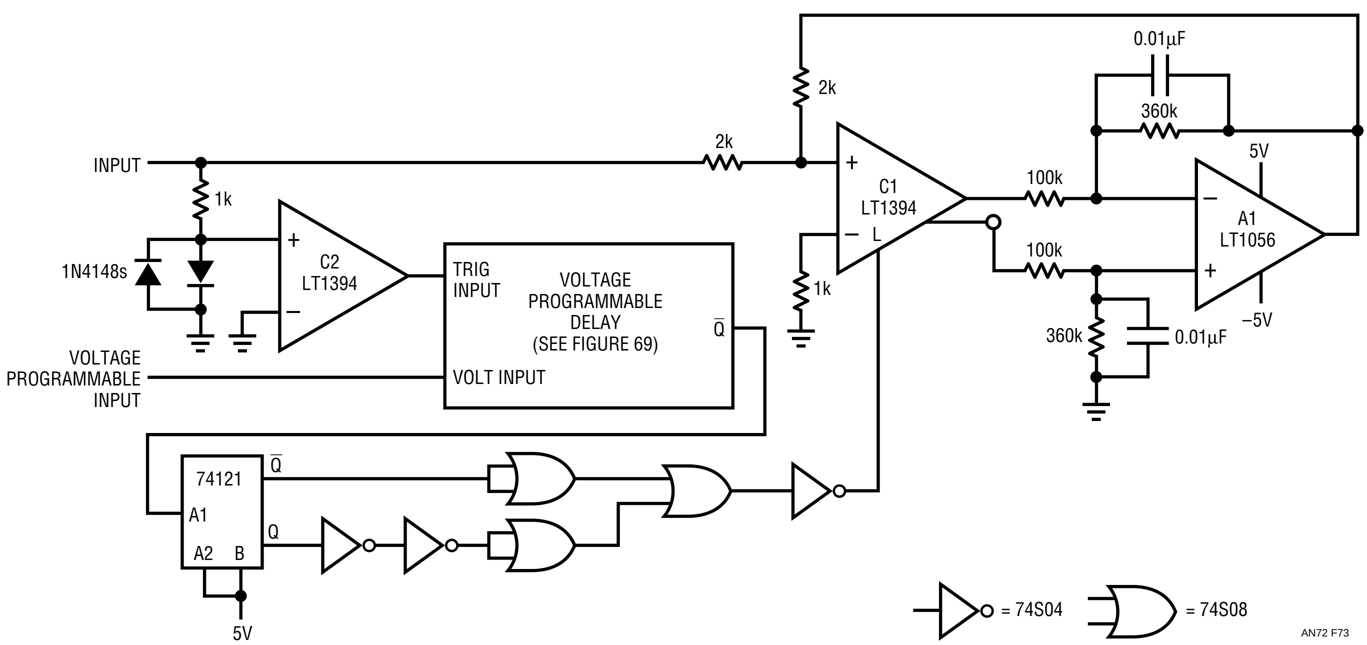



**Figure 73. 10ns Sample-and-Hold for Repetitive Signals. Feedback Loop Around Comparator and Programmable Delay Allow Controllable Sampling of Input**

In Figure 75, C1 and Q1 through Q4 form a voltage programmable delay identical to the one described in Figure 69. Q5, the LT1082 switching regulator and associated components comprise the avalanche pulse generator. The generator provides an 800ps pulse with rise and fall times inside 250ps. Pulse amplitude is 10V with a 50Ω source impedance.

The pulse generator requires high voltage bias for operation. The LT1082 switching regulator forms a high voltage switched mode control loop. The LT1082 pulse width modulates at its 40kHz clock rate. L1's inductive events are rectified and stored in the 2μF output capacitor. The adjustable resistor divider provides feedback to the LT1082. The 10k-1μF RC provides noise filtering.

The high voltage is applied to Q5, a 40V breakdown device, via the R3-C1 combination. The high voltage "bias adjust" control should be set at the point where free running pulses across R4 *just* disappear. This puts Q5 slightly below its avalanche point. When C1's output pulse is applied to Q5's base, it avalanches. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges to just below the avalanche point. At C1's next pulse this action repeats[14].

Figure 76 shows the circuit input trigger (Trace A) that initiates the delay. After a time set by the programming input voltage, C1 goes high (Trace B). The avalanche pulse output is indicated in Trace C, but probe and oscilloscope bandwidth limitations prevent an accurate representation.

**Note 14:** This circuit is based on the operation of the Tektronix Type 111 pulse generator. See Reference 20.

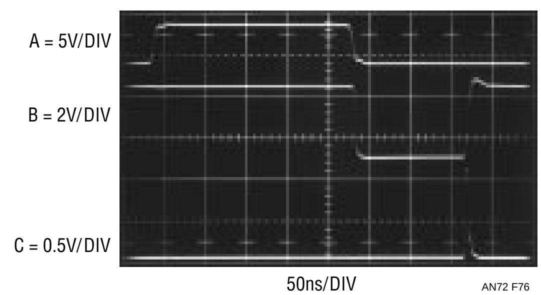



**Figure 76. Input Trigger (Trace A) Initiates Delay (Trace B) with Resultant Output Pulse (Trace C). Oscilloscope Bandwidth Limitations Prevent Accurate Output Pulse Representation**

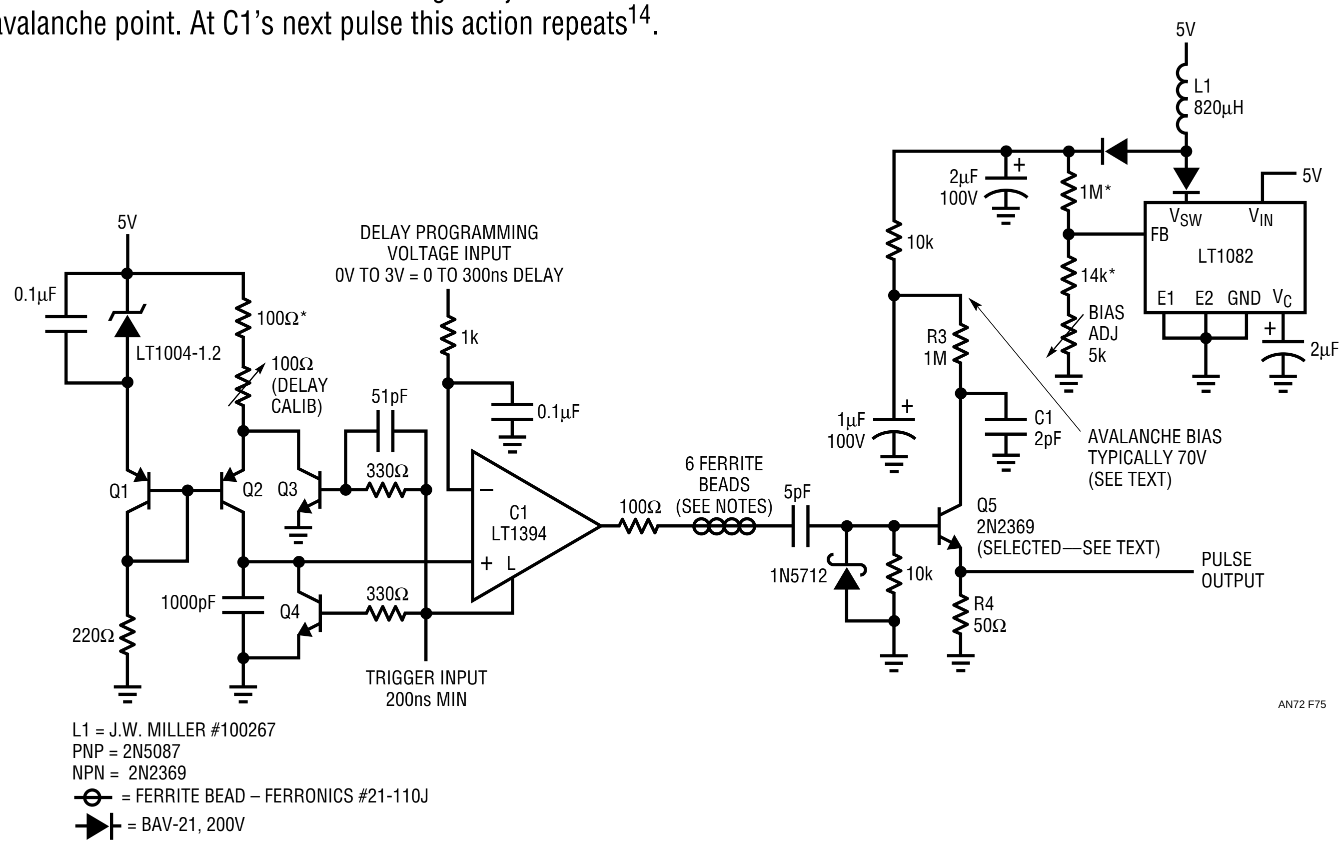



**Figure 75. Figure 69's Programmable Delay Triggers a Sub-Nanosecond Pulse Generator**

Figure 77, taken with a 3.9GHz bandpass instrument (Tektronix 661 with 4S2 sampling plug-in) shows more detail. Trace A is C1's output, and Trace B is the avalanche pulse. When avalanche occurs, Q5's reverse base current rises so abruptly that C1's output cannot directly absorb it. The 100Ω resistor and the ferrite beads present impedance at frequency, allowing C1 to handle the load. Without this network, C1's positive-going output will completely reverse direction and ring severely before completing its transition, corrupting avalanche behavior. Even with these components, artifacts of the avalanche induced base current are clearly visible in C1's trace.

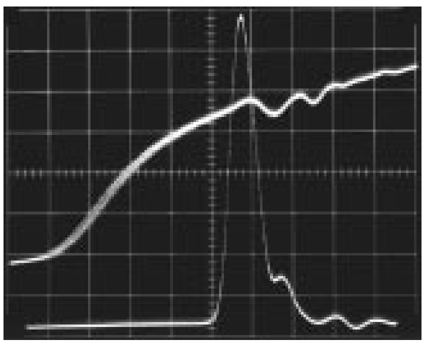



**Figure 77. 3.9GHz Sampling Oscilloscope Measures Delay Output and Avalanche Pulse. Pulse-Induced Loading Is Buffered by Ferrite Beads, but Artifacts Appear in Delay Output**

The avalanche pulse measures 8V high with a 1.2ns base. Rise time is 250ps, with fall time indicating 200ps. The times are probably slightly faster, as the oscilloscope's 90ps rise time influences the measurement.[15]

Q5 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12-year date code span, yielded 82%. All "good" devices switched in less than 600ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout, connection and termination techniques is essential for good results from this circuit.

## Fast Pulse Stretcher

The minimum input pulse width required to operate a pulse stretcher is usually in the 5ns to 10ns range. Additionally, the rise and delay times are of the same order. Figure 78's circuit is considerably faster. It produces a stretched pulse from a 2ns width input with rise and delay times of 650ps.

**Note 15:** I'm sorry, but 3.9GHz is the fastest 'scope in my house (as of November 1996).

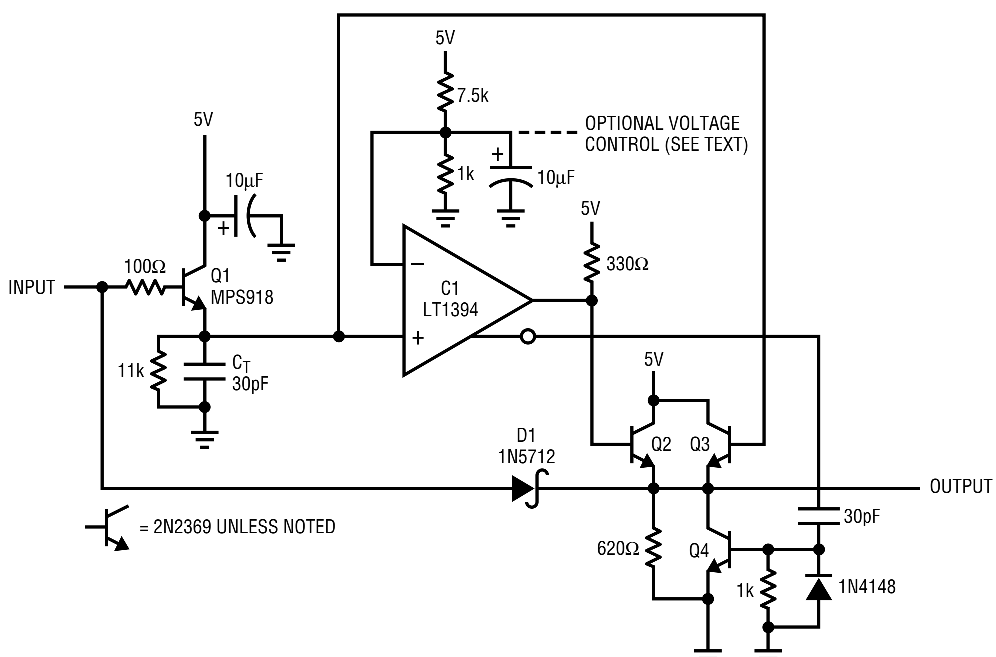



**Figure 78. High Speed Pulse Stretcher Has Sub-Nanosecond Delay and Rise Time**

The input pulse (Trace A, Figure 79) causes Q1 to conduct, charging the timing capacitor, $C_T$ (Trace B). The input pulse is also fed forward around C1, via D1, to the output (Trace C). Additionally, $C_T$'s potential, buffered by Q3, is similarly fed forward to the output. C1 responds to $C_T$'s charging by going high. Its output turns Q2 on, augmenting the outputs high state. C1's 7ns delay does not affect output delay or waveshape because the feedforward paths "fill in" the dead time before the comparator responds. The output pulse is a composite of the input and comparator-based response. The small change in output amplitude when the input ceases is related to this, but is not deleterious. When the input pulse falls, C1's output, and hence the circuits output, remains high until $C_T$ discharges below C1's negative input. When C1 goes low its inverting output goes high, pulsing Q4 to pull the output down in 5ns.

The feedforward paths are crucial to circuit operation. The effect of D1's path is readily understood, but the $C_T$-originated route is less obvious. A good way to see the effect of $C_T$'s path is to eliminate it. Figure 80's photo, taken with Q3's base open, is quite revealing. Trace A is the input pulse, Trace B the output and Trace C is C1's output. The absence of the $C_T$ -based feedforward path is clearly evident. The output (again, Trace B) sags for 8ns before the comparator responds, restoring output amplitude.

Evaluating circuit operation requires a fast pulse generator and a wideband oscilloscope. Figure 81's photo, taken at 100× Figure 79's sweep rate, shows the pulse stretcher's input-output relationship in a 3.9GHz sampled bandpass. Trace A is the input pulse and Trace B the output. As in Figure 79, output amplitude drops slightly when the input ceases, but the logical high state is maintained. Also visible on the inputs leading edge is a 0.5V amplitude 500ps aberration which occurs about 3V into the transition.

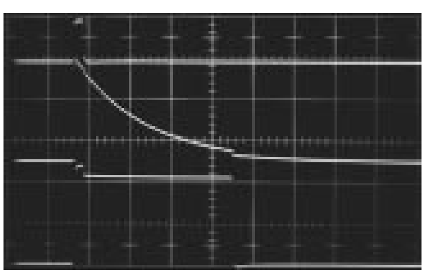



**Figure 79. Waveforms for the Pulse Stretcher. Input (Trace A) Triggers Ramp Decay (Trace B), Resulting in Stretched Output (Trace C). Output Is a Composite of Input and Comparator-Based Response**

Figure 82 further increases sweep rate to examine the input (Trace A) and output (Trace B) leading edges. The output is delayed from the input by only 650ps, with rise time also

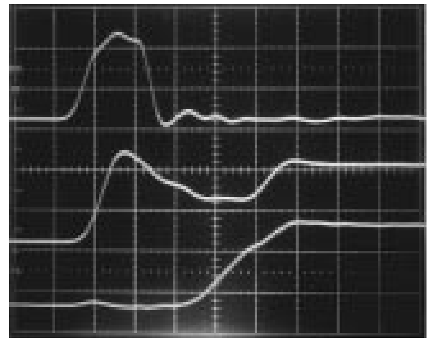



**Figure 80. Results of Disconnecting $C_T$-Originated Feedforward Path. Output (Trace B) Sags for 8ns Before C1 (Trace C) Can Restore Its Amplitude**

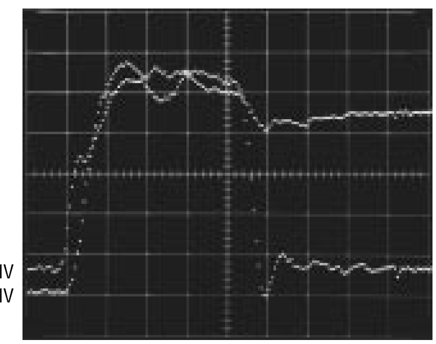



**Figure 81. Pulse Stretchers Input-Output Relationship in a 3.9GHz Bandpass. Output Amplitude Drops When Input Decays, but Logic Level Is Maintained. Sampling Oscilloscope Display Is a Series of Dots**

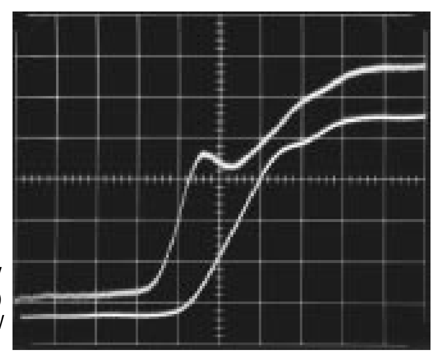



**Figure 82. Pulse Stretcher Waveforms in 3.9GHz Bandpass Show 650ps Output Rise and Delay Times (Trace B). Nonlinear Loading Causes Input Transition Aberration (Trace A), but Is Not Deleterious. Trace Granularity Derives from Sampling Oscilloscope Operation**

about 650ps. The input transition aberration, now clearly visible, is due to the circuits nonlinear input impedance. It occurs above a logical high level, and is acceptable.

Output pulse width is approximately equal to the input pulse width added to 25ns/pF of $C_T$. The ratiometric biasing of C1's inputs provides supply variation immunity from 5V ±5%. The output width can be voltage controlled by biasing C1's negative input, but supply immunity will be compromised. The minimum input trigger width to maintain programmed output width within 1% is 2ns.

### 20ns Response Overvoltage Protection Circuit

It is often desirable to protect an expensive load from supply overvoltage. Overvoltage events may derive from supply failure or poor transient response. In Figure 83, Q1, a source follower, receives gate overdrive bias from the 12V bias supply and is saturated. The regulator driving Q1's drain takes feedback from the source, eliminating Q1's saturation resistance as an output impedance term.

C1 monitors the 3V output feeding the protected load. Under normal conditions C1's positive input is below its negative input, and its output is low. Q2 through Q5 are off and the load receives drive via Q1. Figure 84 shows what happens when an overvoltage event occurs. The 3V output (Trace A) begins to rise (note upward excursion beginning about center screen). This is detected at C1, and its output (Trace B) goes high. Q2 and Q3 come on very quickly, pulling down Q1's gate (Trace C). Q4 and Q5, slower devices, turn on after Q2-Q3, and shunt Q1's residual output to ground without experiencing excessive current. C1's output is fed via a 330Ω resistor to its latch pin. This causes C1 to latch high, preventing any output until the overvoltage cause is corrected. Reset is accomplished by breaking the latch with the normally open reset switch.

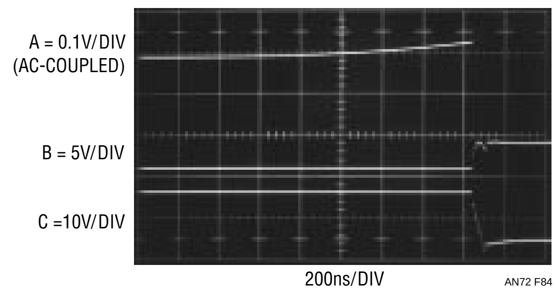



**Figure 84. Overvoltage Event (Note Upward Excursion, Trace A) Triggers Comparator (Trace B), Resulting in Gate Bias Collapse (Trace C)**

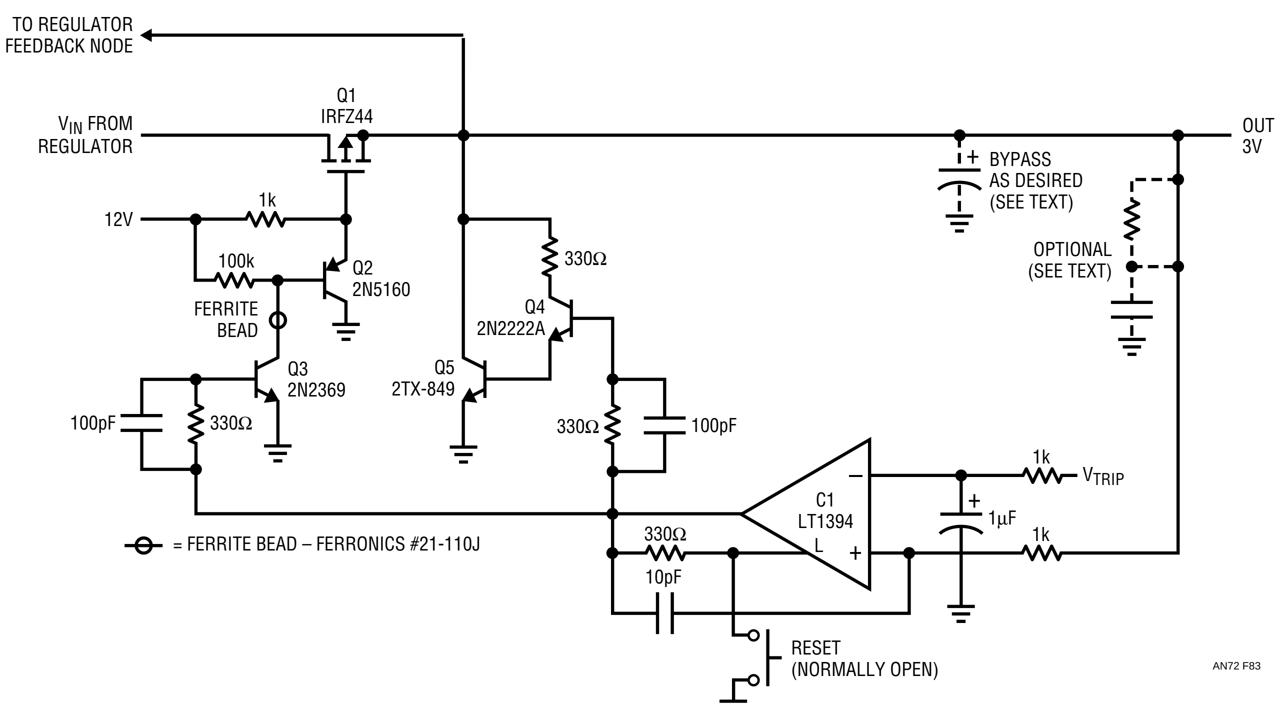



**Figure 83. A 20ns Response Time Overvoltage Protection Circuit. Latching Comparator Drives a Turn-Off Optimized Series—Shunt Switch**

The switching is arranged to optimize turn-off time; Figure 85 shows just how fast the circuit is. As before, Trace A is the 3V output; Trace B, C1's output and Trace C, Q1's gate. The output's amplitude (Trace A) excursion begins just prior to the second vertical division. C1 responds (Trace B) by going high, turning on Q2 and Q3. This initial turn-on pulls Q1's gate downwards (Trace C), arresting the output excursion in 20ns. As Q2 pulls charge out of Q1, gate bias decays. When Q4 and Q5 come on, Q1 is out of saturation and the output drops rapidly. The overvoltage event is arrested in 20ns with total shutdown taking 150ns. Bypassing of Q1's source is optional—it will slow down the overvoltage rise time, but also restricts turn-off time. Similarly, the optional RC filter will eliminate noise-induced nuisance tripping at the expense of response time.

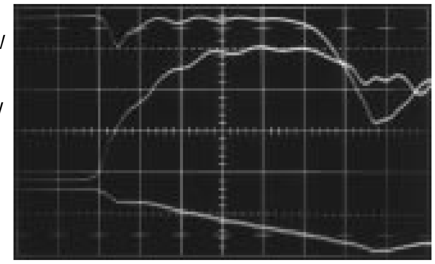



**Figure 85. Detail of Protection Circuits Behavior. Output Amplitude Excursion (Trace A) Triggers Comparator (Trace B), Resulting Gate Drive Removal (Trace C). Overvoltage is Arrested in 20ns, Complete Shutdown Requires 150ns**

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## APPENDIX A

### About Level Shifts

The LT1394's logic output will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1394-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1394 is a sink-source pair (Figure A1) with good ability to drive capacitance (such as feedforward capacitors). Figure A2 shows a noninverting voltage gain stage with a 15V output. When the LT1394 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low impedance output and the Schottky diode aids current sink capability.

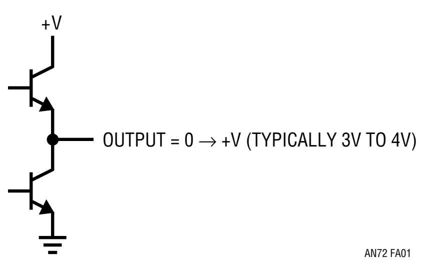


**Figure A1. Simplified LT1394 Output Stage**

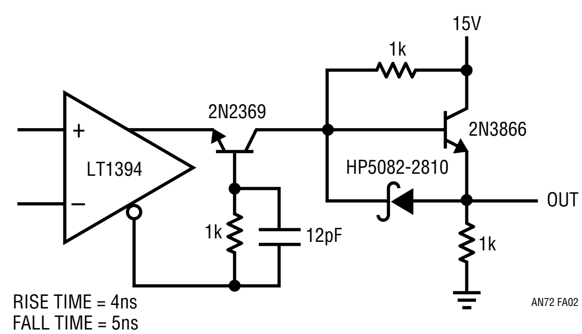


**Figure A2. Level Shift Has Noninverting Voltage Gain**

Figure A3 is a very versatile stage. It features a bipolar swing that is set by the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1394 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1394's output transition (Trace A, Figure A5), but Q2's switching is clean (Trace B, Figure A5) with 3ns delay on the rise and fall of the pulse. Figure A4 is similar to A2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET that switches 1A at 15V. Most of the 7ns to 9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high $f_T$s. To get the kind of results shown, switching times in the nanosecond range and $f_T$s approaching 1GHz are required.

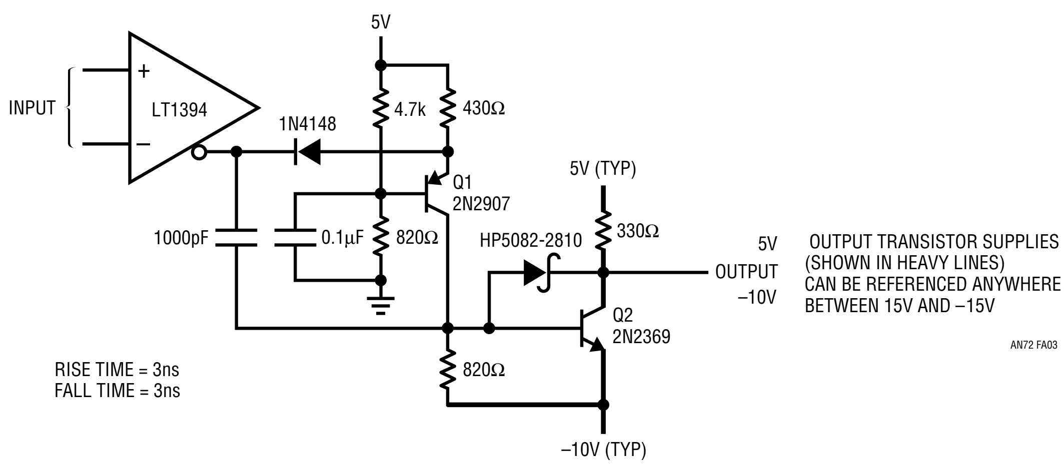


**Figure A3. Level Shift with Inverting Voltage Gain—Bipolar Swing**

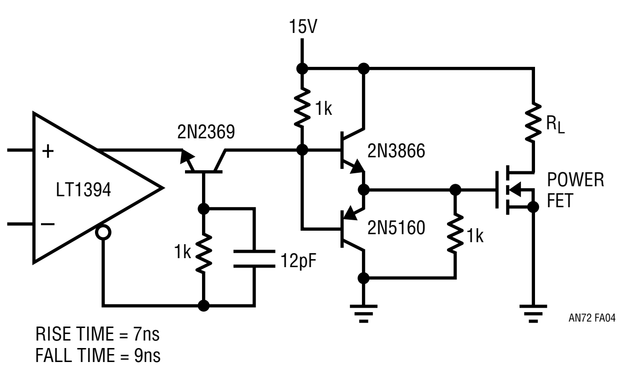


**Figure A4. Noninverting Voltage Gain Level Shift**

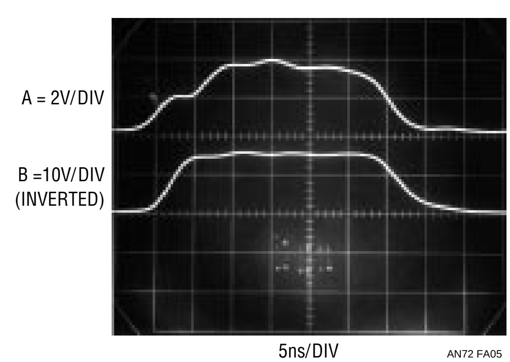


**Figure A5. Figure A3's Waveforms**

## APPENDIX B

### Measuring Probe-Oscilloscope Response

The LT1394's 7ns response time and the circuitry it is used in will challenge the best test equipment. Many of the measurements made utilize equipment near the limit of its capabilities. It is a good idea to verify parameters such as probe and scope rise time and differences in delays between probes and even oscilloscope channels. Verifying the limits of wideband test equipment setups is a difficult task. In particular, the end-to-end rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure B1 circuit does this, providing a 1ns pulse with rise and fall times inside 250ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage step-up network. L1 periodically receives charge and its flyback discharge delivers high voltage events to the step-up network. A portion of the step-up network's DC output is fed back to the LT1073 via the 10M-24k divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the 1M-2pF combination. Q1, a 40V breakdown device, nondestructively avalanches when C1 charges high enough. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free running oscillation at about 200kHz.[1, 2] Figure B2 shows the output pulse. A 12.4GHz sampling oscilloscope measures the double-terminated pulse at 4.8V high with about a 700ps base. Rise time is 216ps, with fall time 232ps. There is a slight hint of ring after the falling edge, but it is well controlled.

**Note 1:** This method of generating fast pulses borrows heavily from the Tektronix type 111 Pretrigger Pulse Generator. See References 17, 20, 22, 27 and 28.
**Note 2:** If desired, the avalanche pulse generator may be externally triggered. See Figure 75 and associated text. See also References 20 and 22.

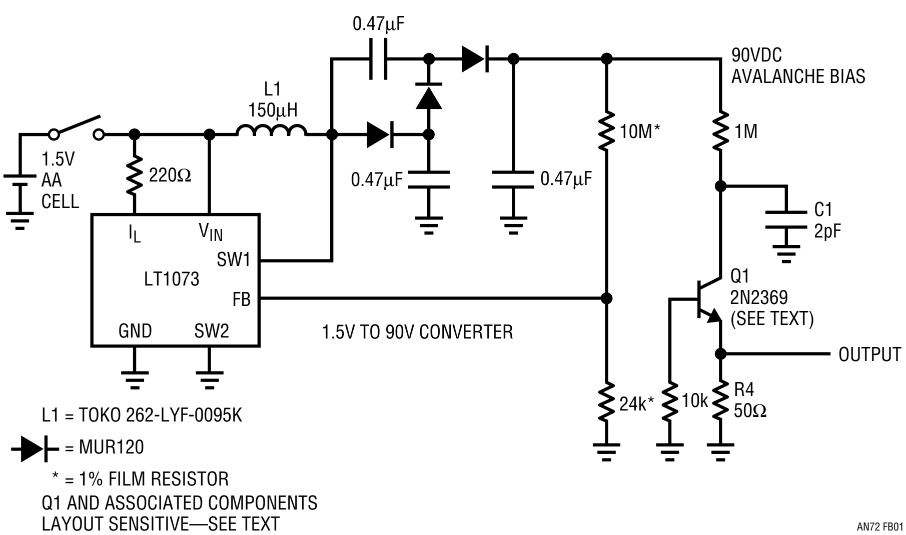


**Figure B1. 250ps Rise/Fall Time Avalanche Pulse Generator**

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12-year date code span, yielded 82%. All good devices switched in less than 650ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout techniques is essential for good results from this circuit. Current drain from the 1.5V battery is about 5mA.

Figure B3 shows the physical construction of the actual generator. Power, supplied from a separate box, is fed into the generator's enclosure via a BNC connector. Q1 is mounted *directly* at the output BNC connector, with grounding and layout appropriate for wideband operation. Lead length, particularly Q1's and C1's, should be experimented with to get best output pulse purity. Figure B4 is the complete unit.

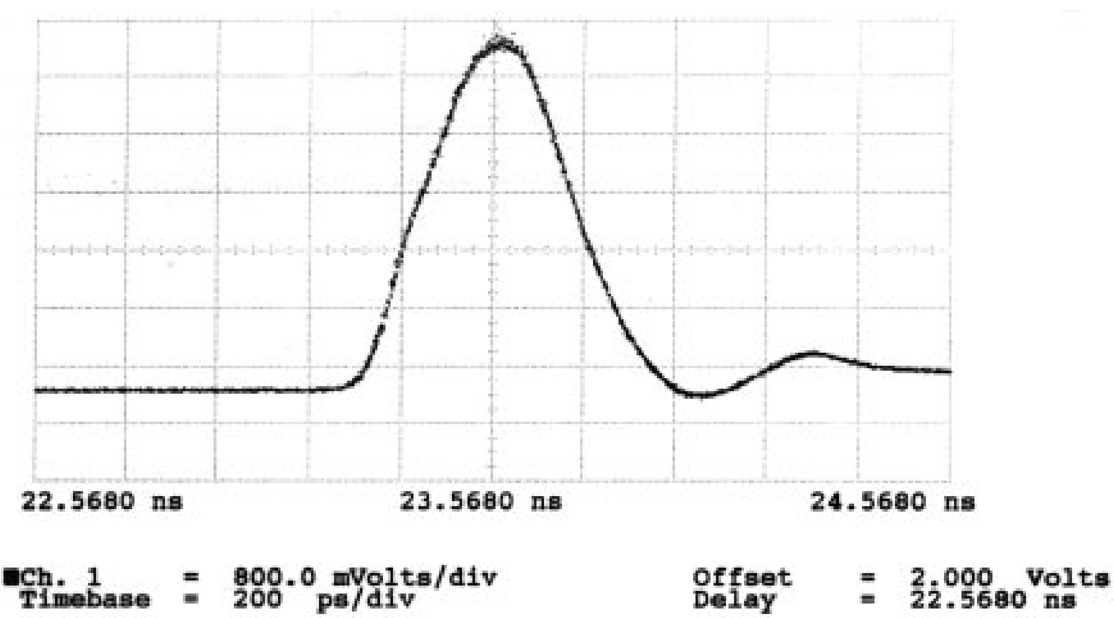


**Figure B2. The Avalanche Pulse Generator's Output Monitored on a Hewlett-Packard 54120B 12GHz Sampling Oscilloscope. Double-Terminated Output Reduces Pulse Amplitude**

(Courtesy of T. Hornak, Hewlett-Packard Laboratories)

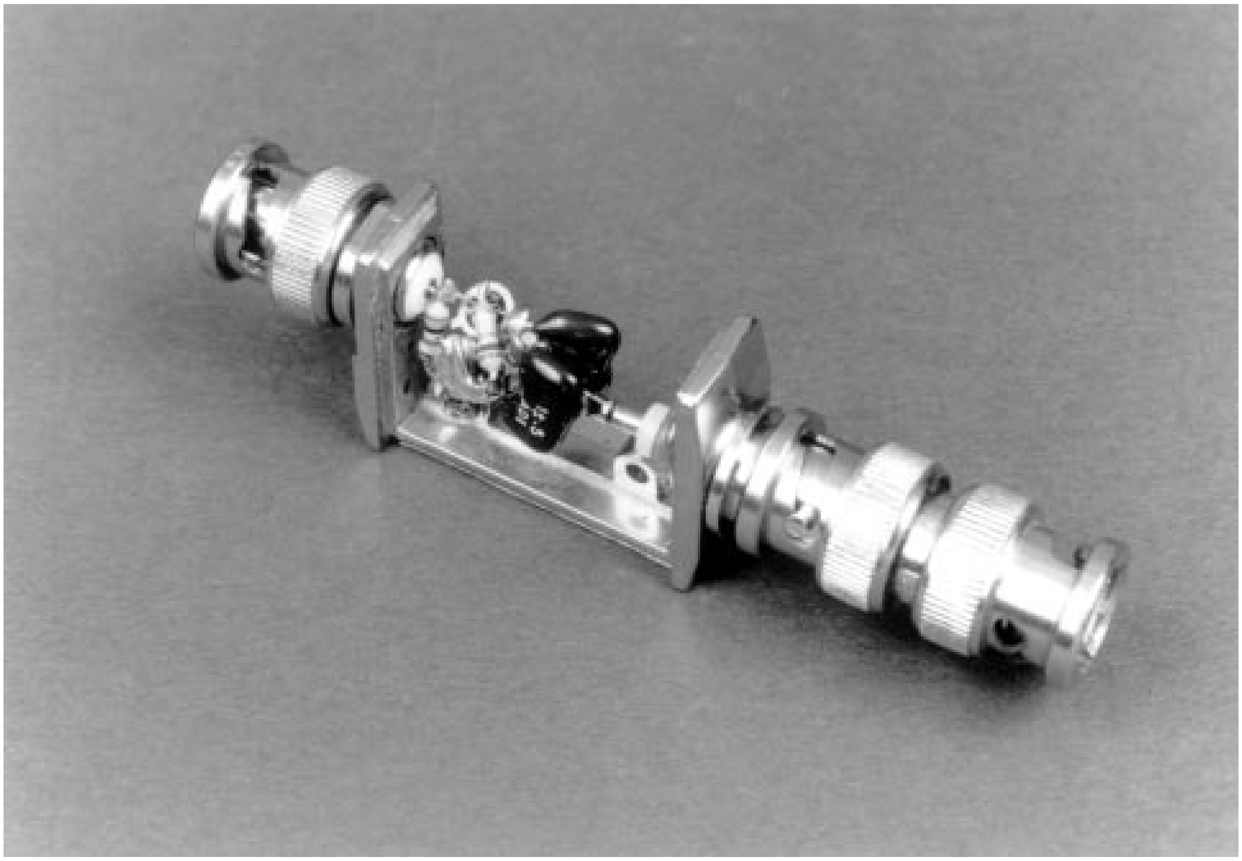

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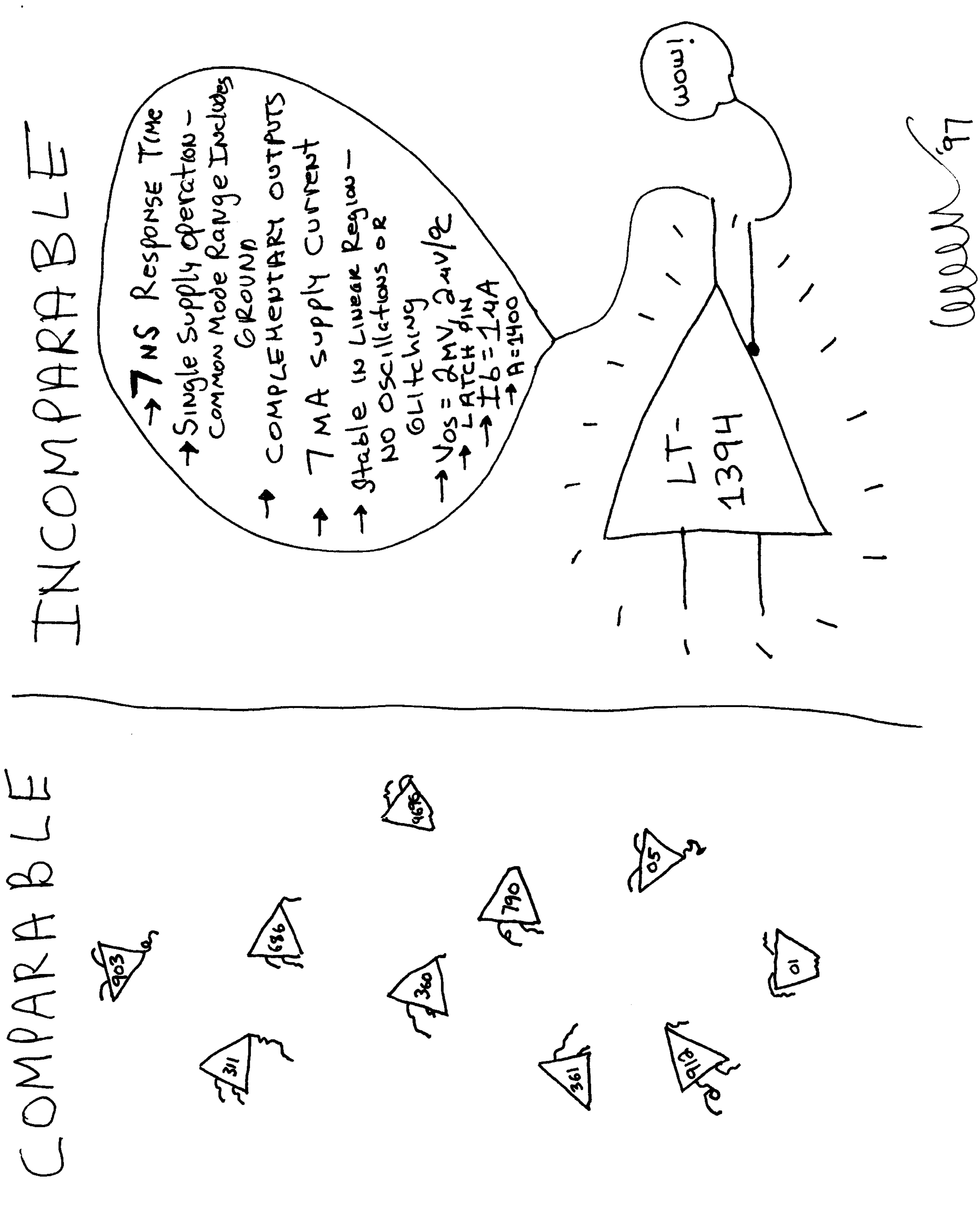
**Figure B3. Details of the Avalanche Pulse Generator's Head. 90VDC Enters at Lower Right BNC, Pulse Exits at Top Left BNC. Note Short Lead Lengths Associated with Output**


AN72 FB04

**Figure B4. The Packaged Avalanche Pulser. 1.5V-to-90V Converter Is in the Black Box. Avalanche Head Is at Left**



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